Total No. of Printed Pages : 4 Roll No.....

MCA-05/PGDCA-05/M.ScIT-05

COMPUTER ORGANIZATION AND ARCHITECTURE

(MCA–11/16/17)

2nd Semester, Examination-2020

Time Allowed : 2 Hours Maximum Marks : 80

Note : This paper is of Eighty (80) marks divided into Two (02) sections A and B. Attempt the question contained in these sections according to the detailed instructions given therein.

Section-A

(Long Answer type Questions)

Note : Section-'A' contains Five (05) Long answer type questions of Twenty (20) marks each. Learners are required to answer any two (02) Questions only. (2×20=40)

1. Explain various elements of cache design and various mapping techniques used with cache.

2. A digital computer has a memory unit of 64*16 and a cache memory of 1 K words. The cache uses direct mapping with a block size of four words. Answer the following questions.

   (a) How many bits are there in the tag, index, block and word fields of the address format?

   (b) How many bits are there in each word of cache and how are they divided into functions? Include a valid bit.

   (c) How many blocks can the cache accommodate?

3. What is Instruction cycle? Explain the phases of an instruction cycle with necessary control functions and micro operations.

4. Explain the difference between hardwired control and micro programmed control. Is it possible to have a hardwired control associated with a control memory?

5. Write short notes on any **three** from the following :

   (a) Virtual memory

   (b) CPU registers

   (c) SISD

   (d) Arithmetic Pipelining.

Section-B

(Short answer type questions)

Note: Section-B Contains Eight (08) Short answer type questions of Ten (10) marks each. Learners are required to answer any four (04) questions only. (4×10=40)

1. What is DMA? Why does DMA have priority over the CPU when both request a memory transfer?

2. Explain the differences between Primary memory and Secondary memory with examples.

3. Explain the various element of bus design.

4. In Cache memory organizations, a write policy like WRITE ONCE, WRITE THROUGH is considered. Why only a WRITE policy and not a READ policy in considered in CACHE memories?

5. List any five memory reference instructions along with their symbolic description.

6. What is an Addressing mode and list the different types?

7. Explain the role of RISC in computer organization and architecture.

8. Explain the role of parallel processing in multi processor organization.

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