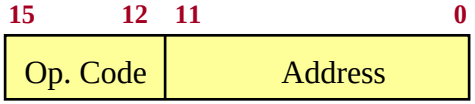
COMPUTER ORGANIZATION

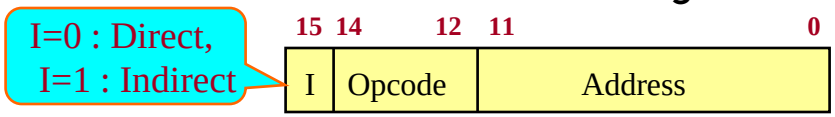
MCA05/MSCIT-05/PGDCA-05/BCA-11

CHAP. 5 BASIC COMPUTER ORG. AND DESIGN

- 5-1 Instruction Codes
  - The user of a computer can control the process by means of a ***program***
  - A program is a sequence of ***instructions*** that specify the operations, operand, the sequence(control)
  - A instruction is a binary code that specifies a sequence of microoperations
  - Instruction codes together with data are stored in memory(=Stored Program Concept)
  - The computer reads each instruction from memory and ***places it in a control register***. The control then ***interprets the binary code*** of the instruction and proceeds to ***execute it*** by issuing a sequence of microoperations.
  - Instruction Code :
    - A group of bits that instruct the computer to perform a specific operation
    - It is usually divided into parts(*refer to Fig. 5-1 instruction format*)
  - Operation Code :
    - The most basic part of an instruction code
    - A group of bits that define such operations as add, subtract, multiply, shift, and complement(*bit 12-15 : 2^4 = 16 distinct operations*)



- Stored Program Organization :
  - The simplest way to organize a computer
    - One processor register : AC(Accumulator)
      - The operation is performed with the memory operand and the content of AC
    - Instruction code format with two parts : Op. Code + Address
      - Op. Code : specify 16 possible operations(4 bit)
      - Address : specify the address of an operand(12 bit)
      - If an operation in an instruction code does not need an operand from memory, the rest of the bits in the instruction(***address field***) can be used for other purpose
      - .Memory : 12 bit = 4096 word(Instruction and Data are stored)
      - Store each instruction code(***program***) and operand (***data***) in 16-bit memory word
- Addressing Mode
  - Immediate operand address :
    - the second part of an instruction code(***address field***) specifies an ***operand***
  - Direct operand address :
    - the second part of an instruction code specifies the ***address of an operand***
  - Indirect operand address :
    - the bits in the second part of the instruction designate an ***address of a memory word in which the address of the operand is found***
  - One bit of the instruction code is used to distinguish between a direct and an indirect address :



- Effective Address
  - The ***operand address*** in *computation-type instruction* or the ***target address*** in a *branch-type instruction*

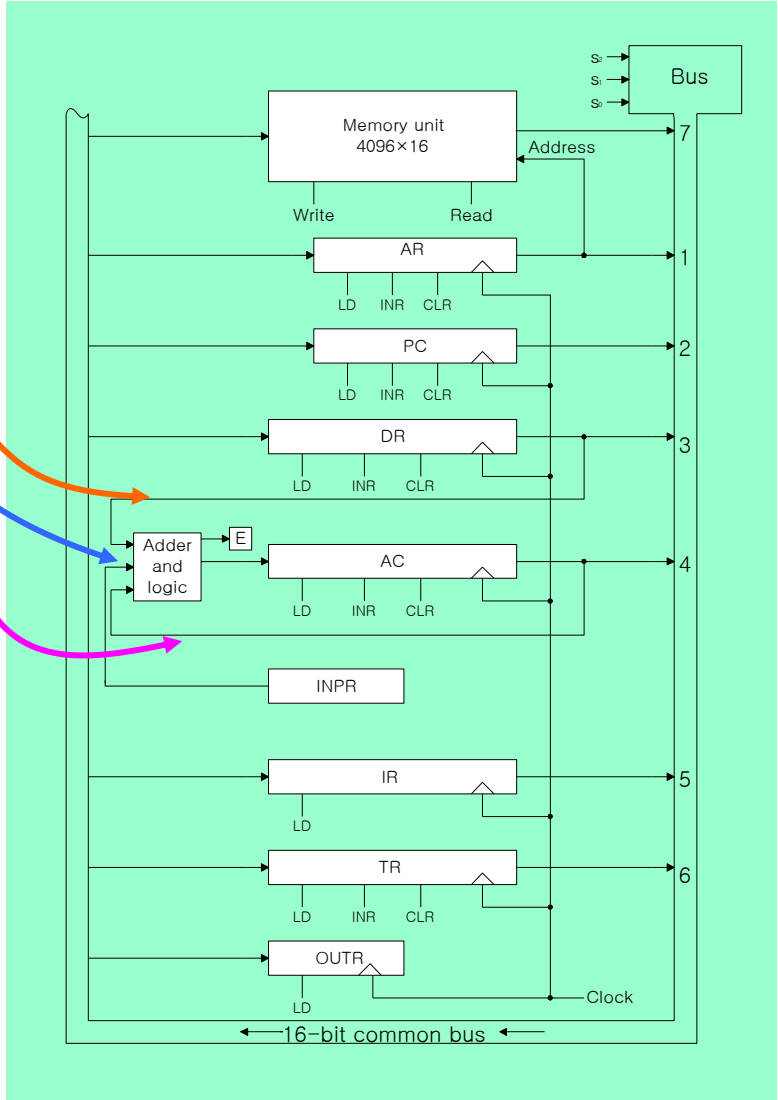
- 5-2 Computer Registers
  - List of Registers for the Basic Computer : ***Tab. 5-1***
  - Basic computer registers and memory : ***Fig. 5-3***
    - Data Register(***DR***) : hold the operand(Data) read from memory
    - Accumulator Register(***AC***) : general purpose processing register
    - Instruction Register(***IR***) : hold the instruction read from memory
    - Temporary Register(***TR***) : hold a temporary data during processing
    - Address Register(***AR***) : hold a memory address, 12 bit width
    - Program Counter(***PC***) :
      - hold the address of the next instruction to be read from memory after the current instruction is executed
      - Instruction words are read and executed in sequence unless a branch instruction is encountered
      - A branch instruction calls for a transfer to a nonconsecutive instruction in the program
      - The address part of a branch instruction is transferred to PC to become the address of the next instruction
      - To read instruction, memory read cycle is initiated, and PC is incremented by one(next instruction fetch)

- Input Register(***INPR***) : receive an 8-bit character from an input device
- Output Register(***OUTR***) : hold an 8-bit character for an output device

- Common Bus System
  - The basic computer has eight registers, a memory unit, and a control unit
  - Paths must be provided to transfer information from one register to another and between memory and registers
  - A more efficient scheme for transferring information in a system with many registers is to use a common bus.
  - The connection of the registers and memory of the basic computer to a common bus system :
    - The outputs of seven registers and memory are connected to the common bus
    - The specific output is selected by mux(S0, S1, S2) :
    - Control Input : LD, INC, CLR, Write, Read
    - Address Register

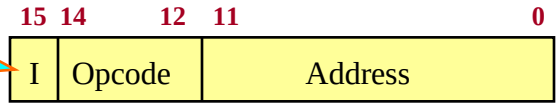
- Accumulator(AC) : 3 Path
  - 1) Register Microoperation : clear AC, shfift AC,…
  - 2) Data Register : **add** DR **to** AC, **and** DR **to** AC(AC End carry bit set/reset), memory READ(DR)
  - 3) INPR
- Note) Two microoperations can be executed at the same time

$$DR \leftarrow AC : s_2 s_1 s_0 = 100(4), DR(load)$$
$$AC \leftarrow DR : DR \rightarrow Adder\ \&\ Logic \rightarrow AC(load)$$



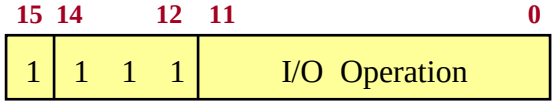
- 5-3 Computer Instruction
  - 3 Instruction Code Formats :
    - Memory-reference instruction
      - Opcode = 000 ~ 110
        - I=0 : 0xxx ~ 6xxx, I=1: 8xxx ~Exxx

I=0 : Direct,
I=1 : Indirect



- Register-reference instruction
  - 7xxx (7800 ~ 7001) : CLA, CMA, ….

- Input-Output instruction
  - Fxxx(F800 ~ F040) : INP, OUT, ION, SKI, ….



Symbol	Hex Code I = 0	Hex Code I = 1	Description
AND	0xxx	8xxx	And memory word to AC
ADD	1xxx	9xxx	Add memory word to AC
LDA	2xxx	Axxx	Load memory word to AC
STA	3xxx	Bxxx	Store content of AC in memory
BUN	4xxx	Cxxx	Branch unconditionally
BSA	5xxx	Dxxx	Branch and Save return address
ISZ	6xxx	Exxx	Increment and skip if zero
CLA	7800		Clear AC
CLE	7400		Clear E
CMS	7200		Complement AC
CME	7100		Complement E
CIR	7080		Circulate right AC and E
CIL	7040		Circulate left AC and E
INC	7020		Increment AC
SPA	7010		Skip next instruction if AC positive
SNA	7008		Skip next instruction if AC negative
SZA	7004		Skip next instruction if AC zero
SZE	7002		Skip next instruction if E is 0
HLT	7001		Halt computer
INP	F800		Input character to AC
OUT	F400		Output character from AC
SKI	F200		Skip on input flag
SKO	F100		Skip on output flag
ION	F080		Interrupt On
IOF	F040		Interrupt Off

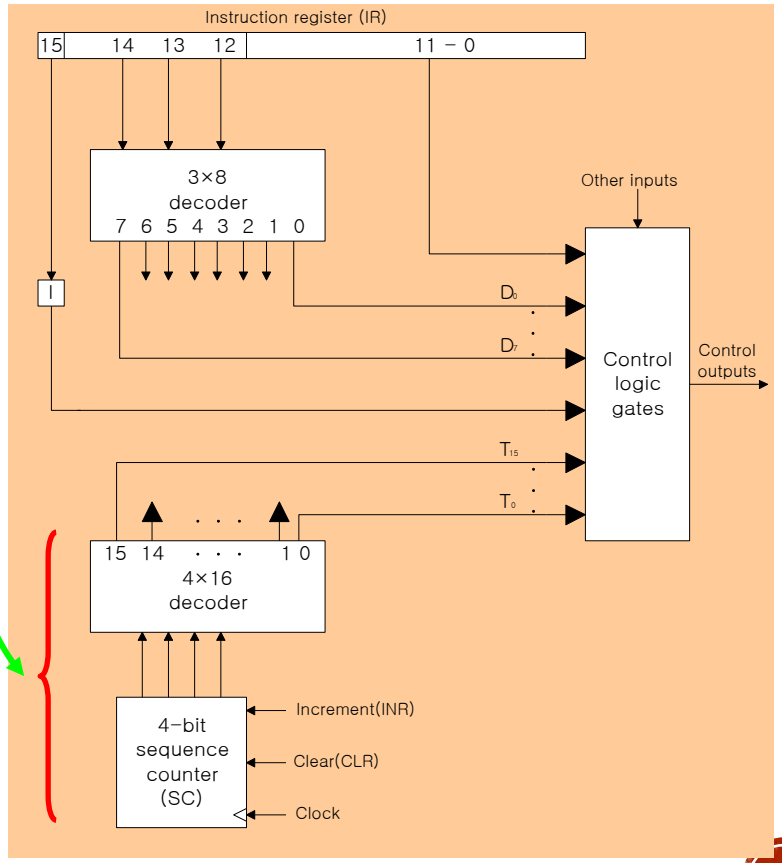
- Instruction Set Completeness
  - Arithmetic, Logical, and shift : CMA, INC, ..
  - Moving information to and from memory and AC : STA, LDA
  - Program control : BUN, BSA, ISZ
  - Input/Output : INP, OUT

- 5-4 Timing and Control
  - Clock pulses
    - A master clock generator controls the timing for all registers in the basic computer
    - The clock pulses are applied to all F/Fs and registers in system
    - The clock pulses do not change the state of a register unless the register is enabled by a control signal
    - The control signals are generated in the control unit :
      - The control signals provide control inputs for the multiplexers in the common bus, control inputs in processor registers, and microoperations for the accumulator
  - Two major types of control organization
    - Hardwired Control :
      - The control logic is implemented with gates, F/Fs, decoders, and other digital circuits
      - + Fast operation, - Wiring change(if the design has to be modified)

- Microprogrammed Control :
  - The control information is stored in a control memory, and the control memory is programmed to initiate the required sequence of microoperations
  - + Any required change can be done by updating the microprogram in control memory, - Slow operation

Control Unit :

- Control Unit = Control Logic Gate + 3 X 8 Decoder + Instruction Register + Timing Signal
- Timing Signal = 4 X 16 Decoder + 4-bit Sequence Counter
- Exam) Control timing :
  - » Sequence Counter is cleared when D_3T_4 =1 : $D_3T_4 : SC \leftarrow 0$
- Memory R/W cycle time > Clock cycle time
  - » wait cycle.



- Exam) Register transfer statement :
  - A transfer of the content of PC into AR if timing signal T_0 is active
    - 1) During T_0 active, the content of PC is placed onto the bus
    - 2) LD(load) input of AR is enabled, the actual transfer occurs at the next positive transition of the clock(*T_0 rising edge clock*)
    - 3) SC(sequence counter) is incremented :

- 5-5 Instruction Cycle
  - Instruction Cycle
    - 1) Instruction Fetch from Memory
    - 2) Instruction Decode
    - 3) Read Effective Address(if indirect addressing mode)
    - 4) Instruction Execution
    - 5) Go to step 1) : Next Instruction[PC + 1]
  - Instruction Fetch : T0, T1

$$T_0 : AR \leftarrow PC$$
$$T_1 : IR \leftarrow M[AR],\ PC \leftarrow PC + 1$$

    - T0 = 1
      - 1) Place the content of PC onto the bus by making the bus selection inputs $S_2S_1S_0$=010
      - 2) Transfer the content of the bus to AR by enabling the LD input of AR

- T1 = 1 $T_1 : IR \leftarrow M[AR], PC \leftarrow PC + 1$
  - 1) Enable the read input memory
  - 2) Place the content of memory onto the bus by making $S_2S_1S_0$= 111
  - 3) Transfer the content of the bus to IR by enable the LD input of IR
  - 4) Increment PC by enabling the INR input of PC

Instruction Decode : T2

$T_2 : D_0,....,D_7 \leftarrow Decode\ IR(12-14),\ AR \leftarrow IR(0-11),\ I \leftarrow IR(15)$

Op.code **Address** **Di/Indirect**

Instruction Execution : T3, T4, T5, T6

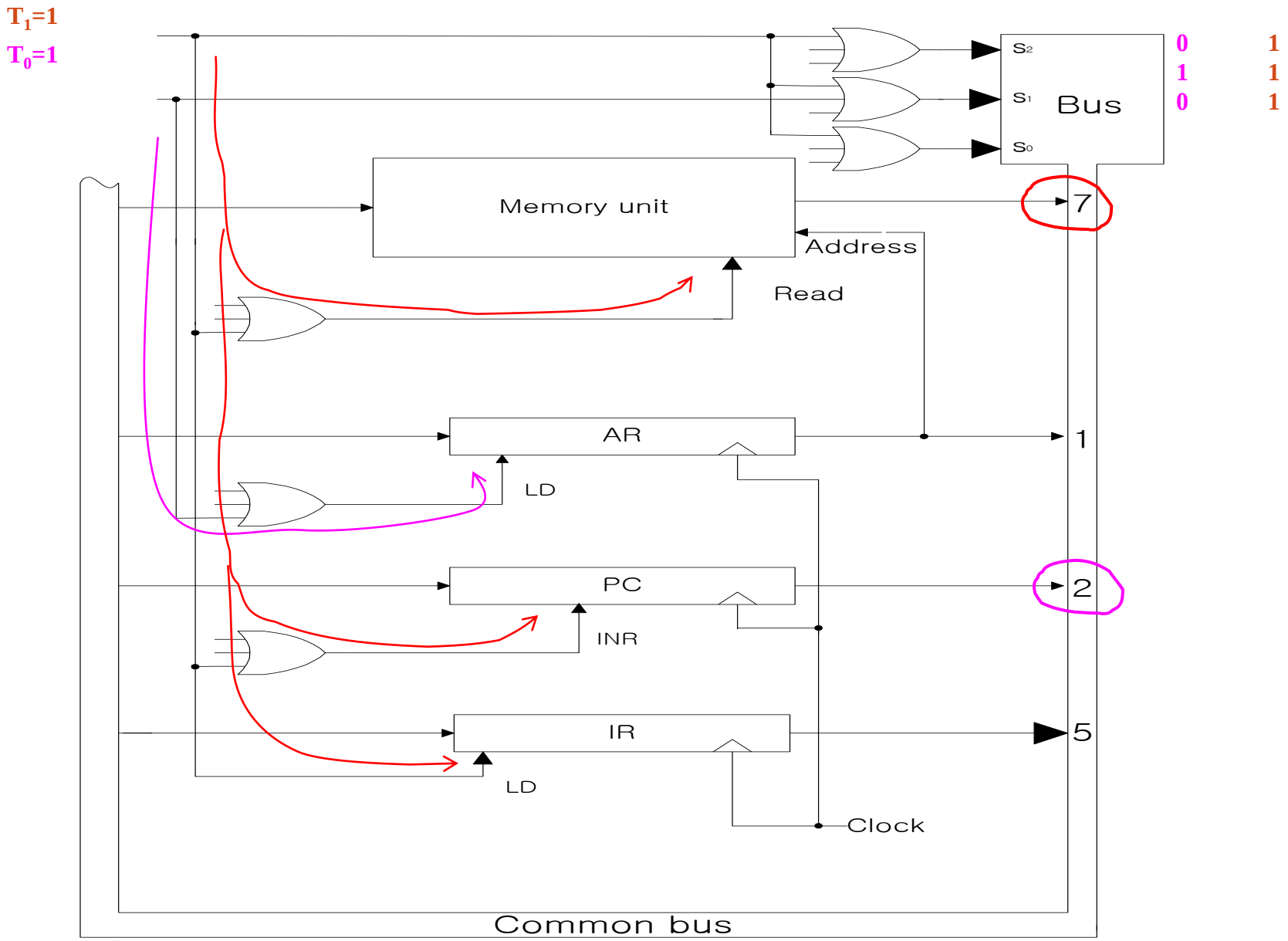
$IR(12-14) = 111$

- D_7=1
  - Register(I=0) → $D_7I'T_3$(Execute)
  - I/O (I=1) → D_7IT_3 (Execute)
- D_7=0 : Memory Ref.
  - Indirect(I=1) → $D_7'IT_3$($AR \leftarrow M[AR]$)
  - Direct (I=0) → nothing in T_3

Read effective Address

- **Register Memory Ref Operand effective address**
- ***Memory Ref.***

Flowchart for instruction cycle(Initial Configuration) :


T1=1
T0=1
S2
S1
S0
Bus
0 1
1 1
0 1
Memory unit
7
Address
Read
AR
1
LD
PC
2
INR
IR
5
LD
Clock
Common bus

- Register Ref. Instruction
  - r = $D_7 I' T_3$:
  - IR(i) = B_i IR(0 -11)
  - ***B_0 - B_{11}*** : **12 Register Ref. Instruction (*Tab. 5-3*)**

Address

- 5-6 Memory Ref. Instruction

D_7 : Register or I/O = 1

3 X 8 Decoder

D_0 : **7 Memory Ref. Instruction(*Tab. 5-4*)**

IR(12,13,14) = 111

- AND to AC

$$D_0T_4 : DR \leftarrow M[AR]$$
$$D_0T_5 : AC \leftarrow AC \wedge DR, SC \leftarrow 0$$

- ADD

$$D_1T_4 : DR \leftarrow M[AR]$$
$$D_1T_5 : AC \leftarrow AC + DR, E \leftarrow C_{out}, SC \leftarrow 0$$

- LDA

$$D_2T_4 : DR \leftarrow M[AR]$$
$$D_2T_5 : AC \leftarrow DR, SC \leftarrow 0$$

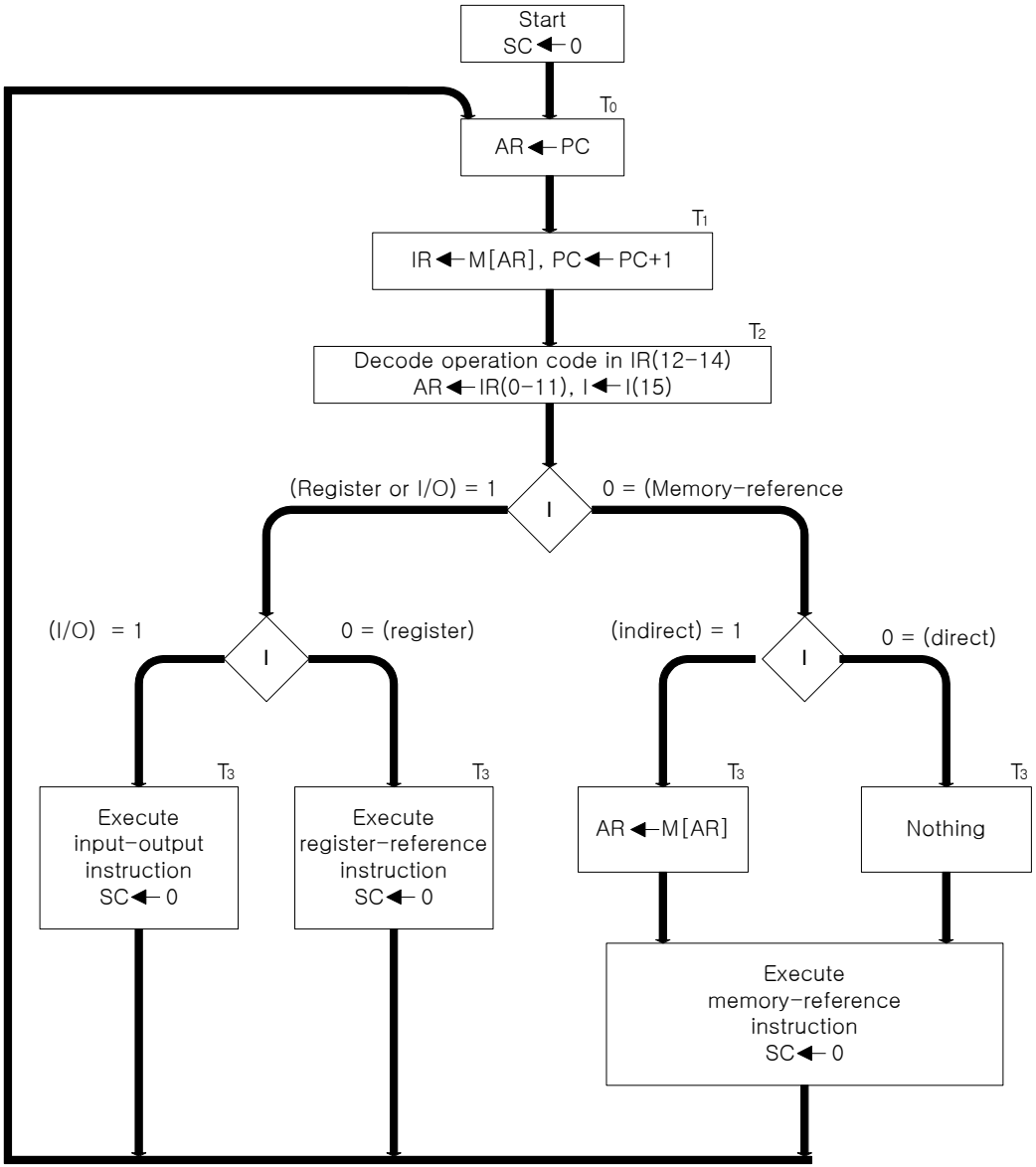
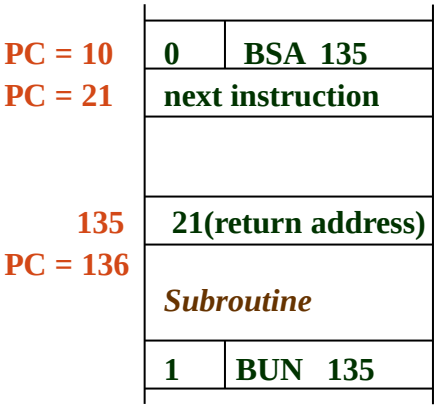

Start
SC ← 0
T0
AR ← PC
T1
IR ← M[AR], PC ← PC+1
T2
Decode operation code in IR(12-14)
AR ← IR(0-11), I ← I(15)
(Register or I/O) = 1
I
0 = (Memory-reference
(I/O) = 1
I
0 = (register)
(indirect) = 1
I
0 = (direct)
T3
Execute input-output instruction
SC ← 0
T3
Execute register-reference instruction
SC ← 0
T3
AR ← M[AR]
T3
Nothing
Execute memory-reference instruction
SC ← 0

Fig. 5-10 Example of BSA



- STA : memory write

  $D_3T_4 : M[AR] \leftarrow AC, SC \leftarrow 0$

- BUN : branch unconditionally

  $D_4T_4 : PC \leftarrow AR, SC \leftarrow 0$

- BSA : branch and save return address

  $D_5T_4 : M[AR] \leftarrow PC, AR \leftarrow AR + 1$

  $D_5T_5 : PC \leftarrow AR, SC \leftarrow 0$

  - Return Address : save return address (135
  - Subroutine Call : *Fig. 5-10*

$D_5T_4 : M[135] \leftarrow 21(PC), 136(AR) \leftarrow 135 + 1$

$D_5T_5 : 136(PC) \leftarrow 136(AR), SC \leftarrow 0$

- $D_6T_4 : DR \leftarrow M[AR]$

  $D_6T_5 : DR \leftarrow DR + 1$

  $D_6T_6 : M[AR] \leftarrow DR, if\ (DR = 0)\ then\ (PC \leftarrow PC + 1), SC \leftarrow 0$

- Control Flowchart :
  - Flowchart for the 7 memory reference instruction
    - The longest instruction : ISZ(T6)
    - 3 bit Sequence Counter)

- 5-7 Input-Output and Interrupt
  - Input-Output Configuration :
    - Input Register(***INPR***), Output Register(***OUTR***)
      - These two registers communicate with a communication interface serially and with the AC in parallel
      - Each quantity of information has eight bits of an alphanumeric code

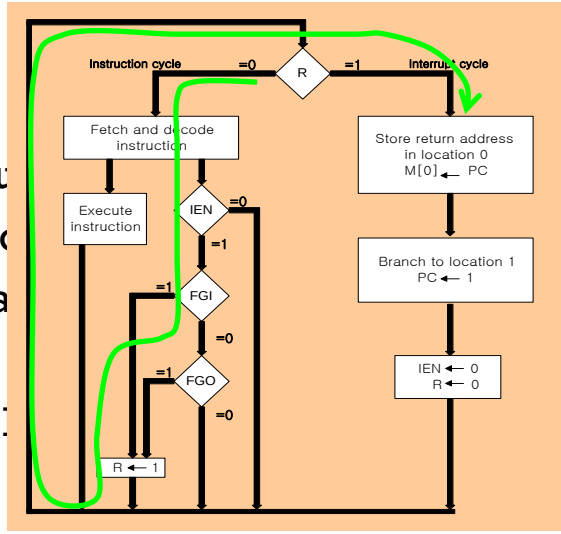
1 : Ready
0 : Not ready

    - Input Flag(***FGI***), Output Flag(***FGO***)
      - FGI : ***set*** when INPR is ready, ***clear*** when INPR is empty
      - FGO : ***set*** when operation is completed, ***clear*** when output device is in the process of printing
  - Input-Output Instruction : *Tab. 5*

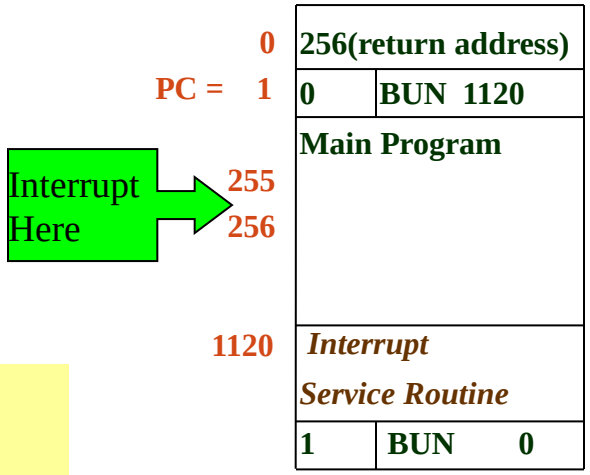
Address

    - p = D_7IT_3
    - IR(i) = B_i IR(6 -11)
    - ***B_6 - B_{11}*** : **6 I/O Instruction**
  - Program Interrupt
    - I/O Transfer Modes
      - 1) Programmed I/O, 2) Interrupt-initiated I/O, 3) DMA, 4) IOP
      - 2) Interrupt-initiated I/O
      - Maskable Interrupt Int. mask

- Interrupt Cycle :
  - During the execute phase, IEN is checked by the control
    - IEN = 0 : the programmer does not want to use the interru
      so control continues with the next instruction cyc
    - IEN = 1 : the control circuit checks the flag bit, If either fla
      set to 1, R F/F is set to 1
  - At the end of the execute phase, control checks the value of I
    - R = 0 : instruction cycle
    - R = 1 : Instruction cycle



- Demonstration of the interrupt cycle :
  - The memory location at address 0 as the place for storing the return address
  - Interrupt Branch to memory location 1
  - Interrupt cycle $T_0'T_1'T_2'(IEN)(FGI + FGO) : R \leftarrow 1$
- The condition for R = 1



- Modified Fetch Phase
  - Modified Fetch and Decode Phase

$$RT_0 : AR \leftarrow 0, TR \leftarrow PC$$
$$RT_1 : M[AR] \leftarrow TR, PC \leftarrow 0$$
$$RT_2 : PC \leftarrow PC + 1, IEN \leftarrow 0, R \leftarrow 0, SC \leftarrow 0$$

REFERENCE

- *Mano, M. Morris (October 1992). Computer System Architecture (3rd ed.). Prentice-Hall. ISBN 0-13-175563-3*
- *Lecture notes of* Dept. of Info. & Comm., Korea Univ. of Tech. & Edu., Korea