Practical : NPN/PNP Transistor

By

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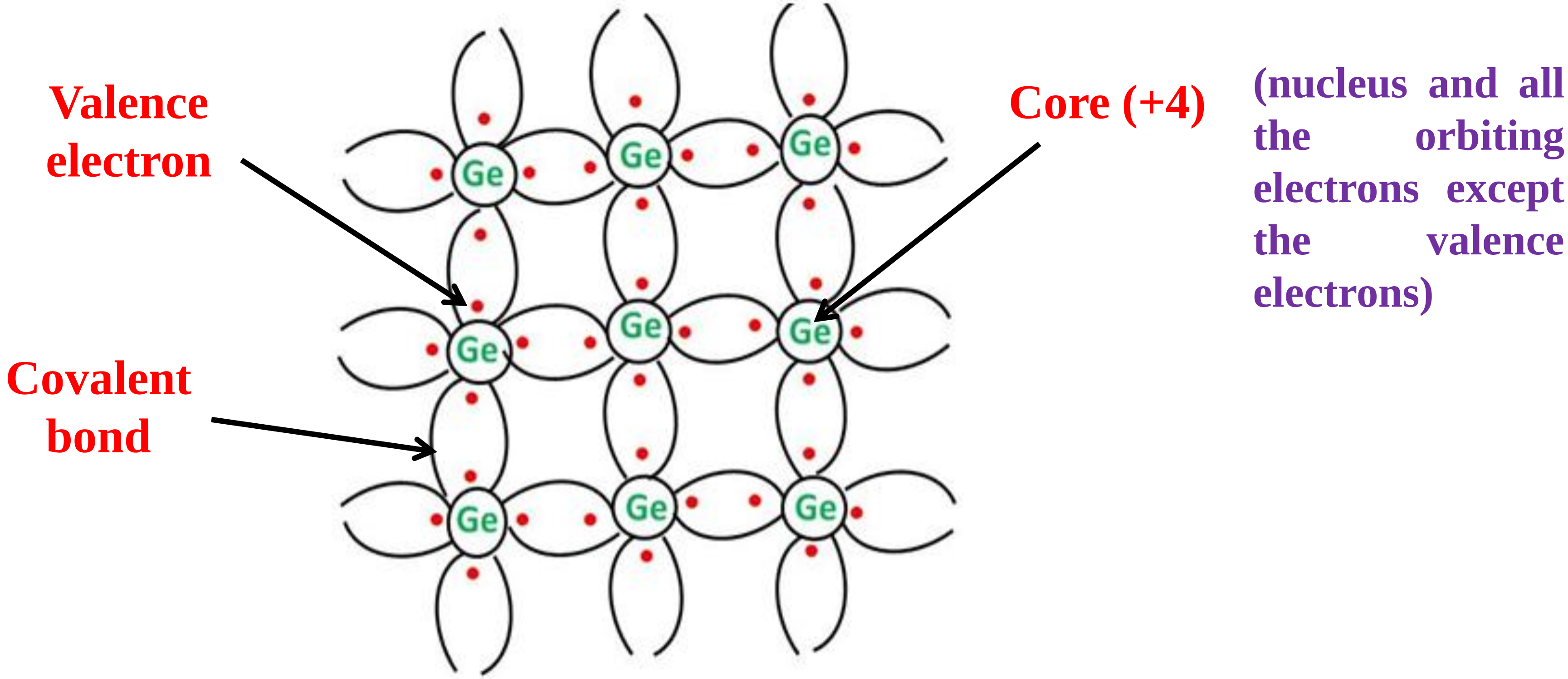
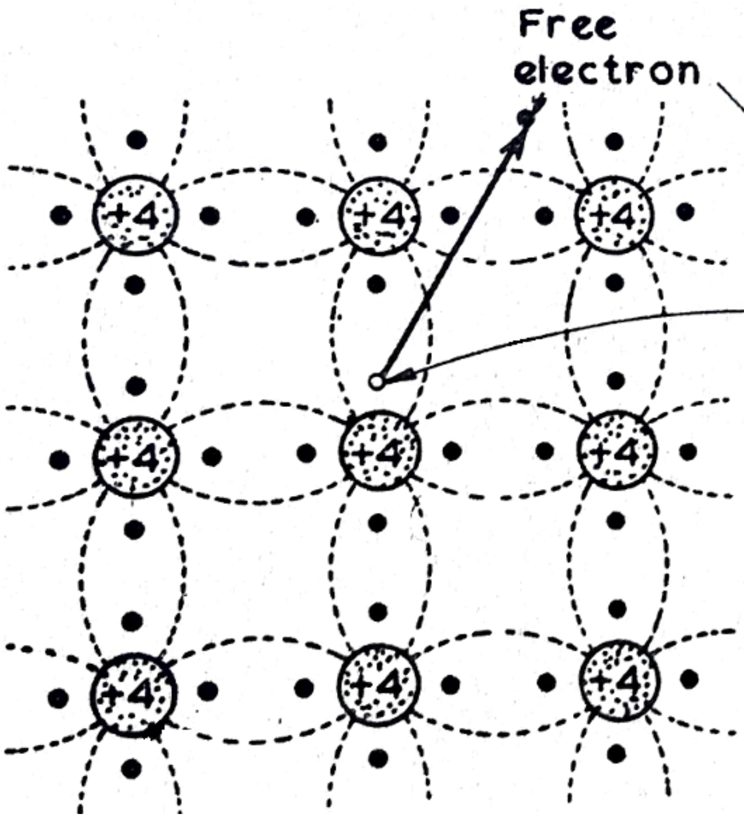


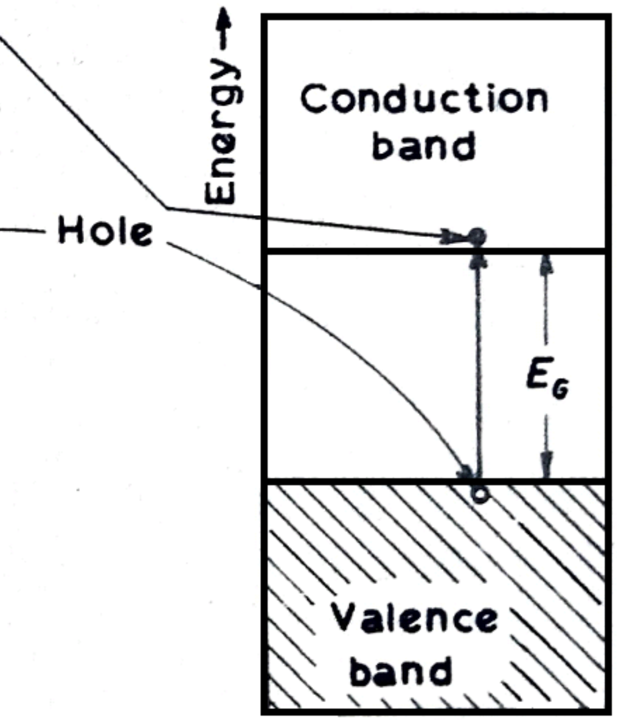
Simplified representation of the crystalline structure of a intrinsic semiconductor (Ge) **[impurity content is less than one part impurity in 100 million parts of semiconductor]** **at absolute zero.**

- At absolute zero, all the valence electrons are tightly bound to the parent atoms. No free electrons are available for electrical conduction. The semiconductor therefore behaves as a perfect insulator at absolute zero.

But what happens at room temperature ?



Crystal structure



Energy-band diagram

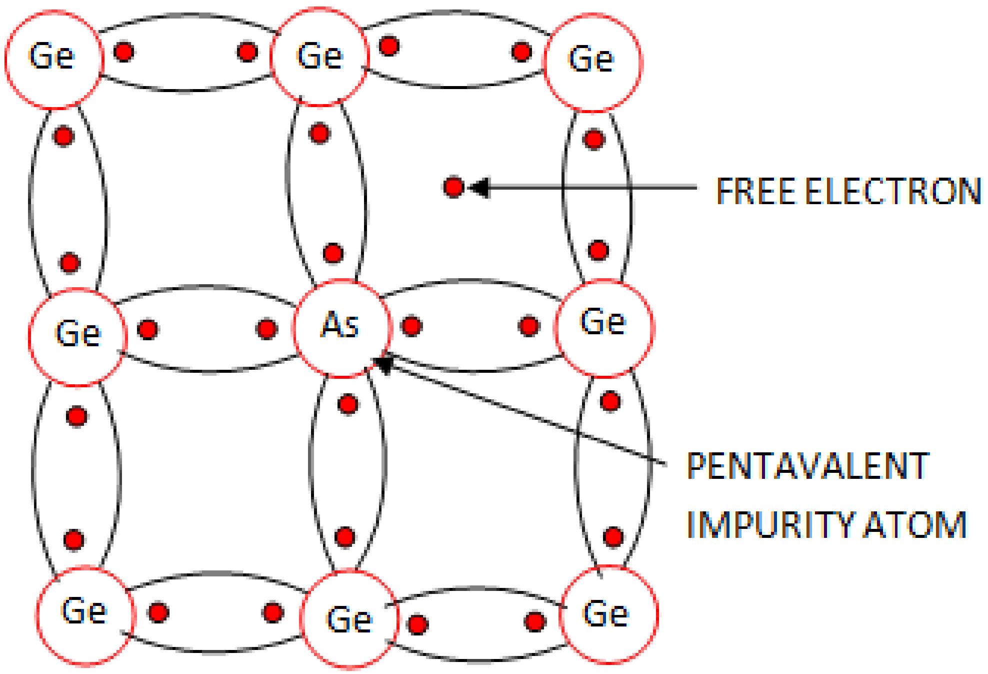
For silicon,
E_g = 1.12 eV

For germanium
E_g = 0.72 eV

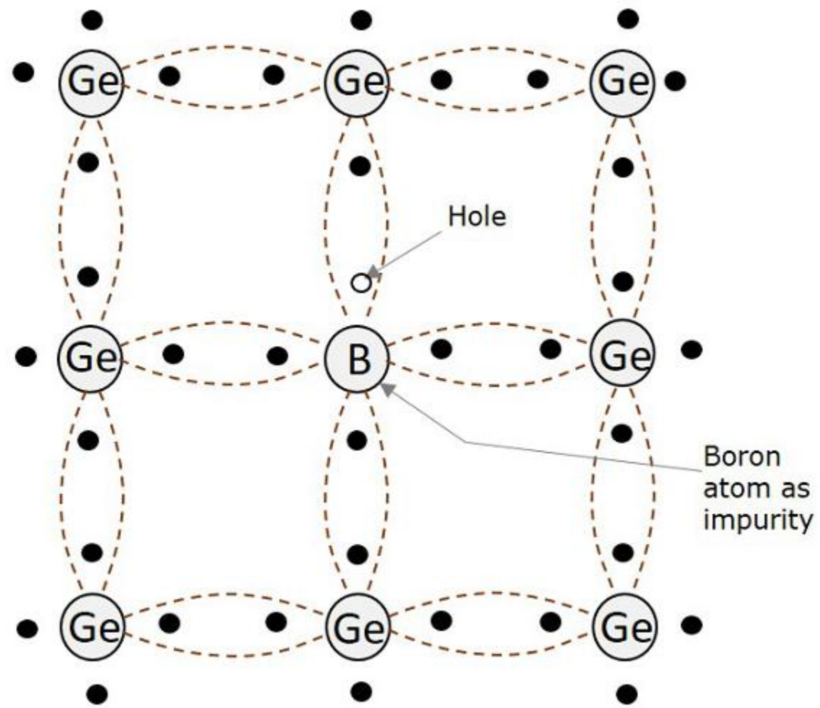
Generation of electron-hole par in an intrinsic semiconductor

❖ Free electrons and holes are always generated in pairs, i.e., concentration of free electrons and holes will always be equal in an intrinsic semiconductor – **Thermal Generation**

Extrinsic semiconductor- The process of deliberately adding impurities (1 atom per 10^8 semiconductor atom) to a semiconductor material is called ***doping***. A doped semiconductor is called ***extrinsic semiconductor***.



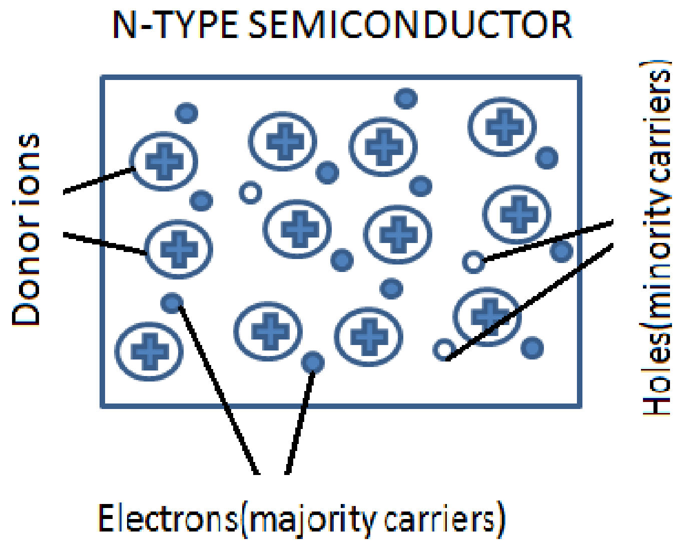
N-Type semiconductor



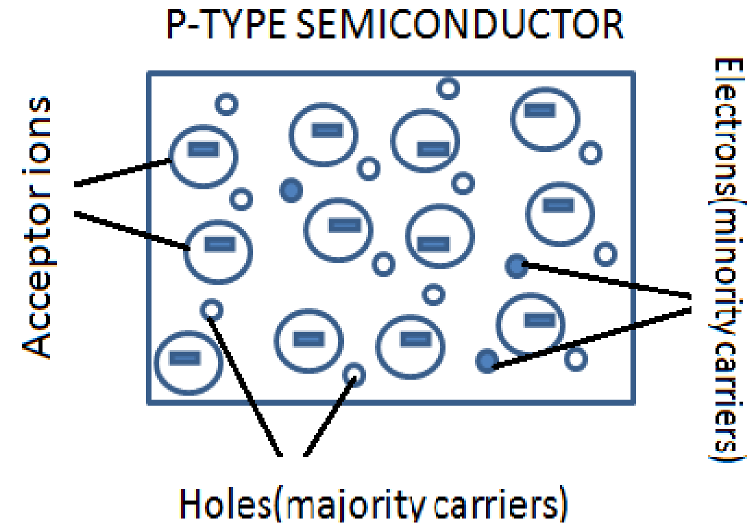
P-Type semiconductor

For N- Type semiconductor: Pentavalent impurities - Arsenic, Antimony, phosphorus (donor impurities)

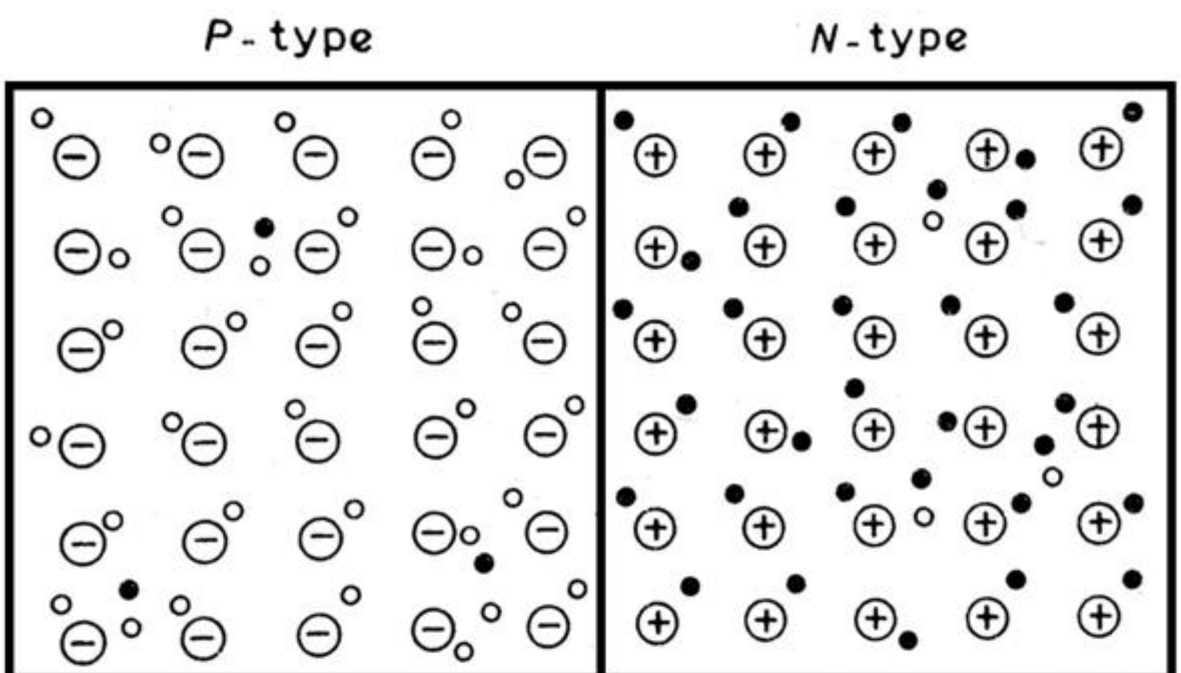
For P- Type semiconductor: Trivalent impurities - Gallium, Indium, boron (acceptor impurities)

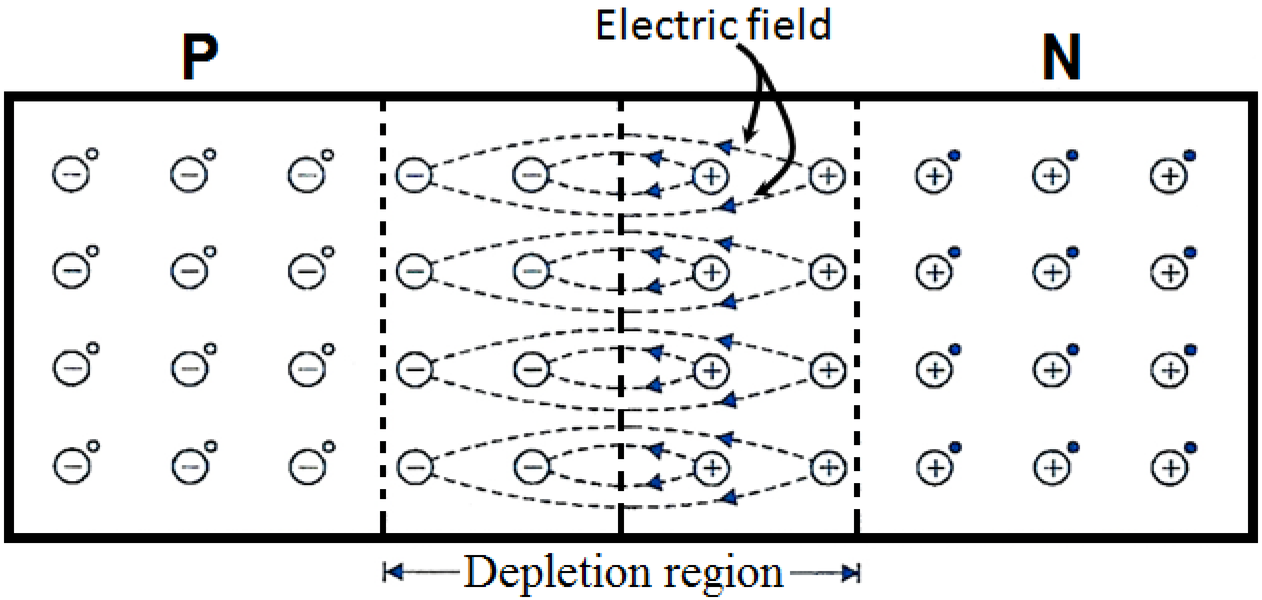


Representation of N-type and P-type semiconductor

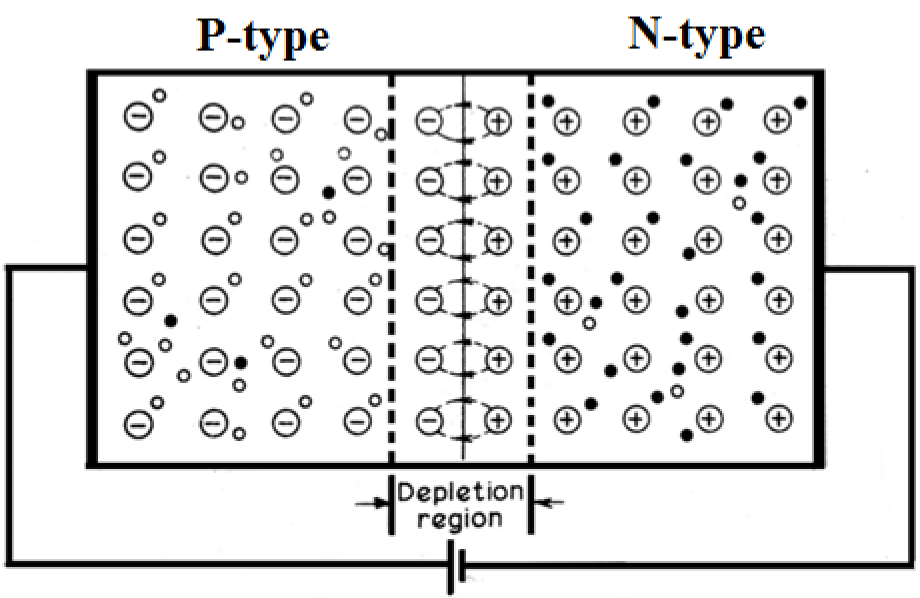


PN-junction when just formed

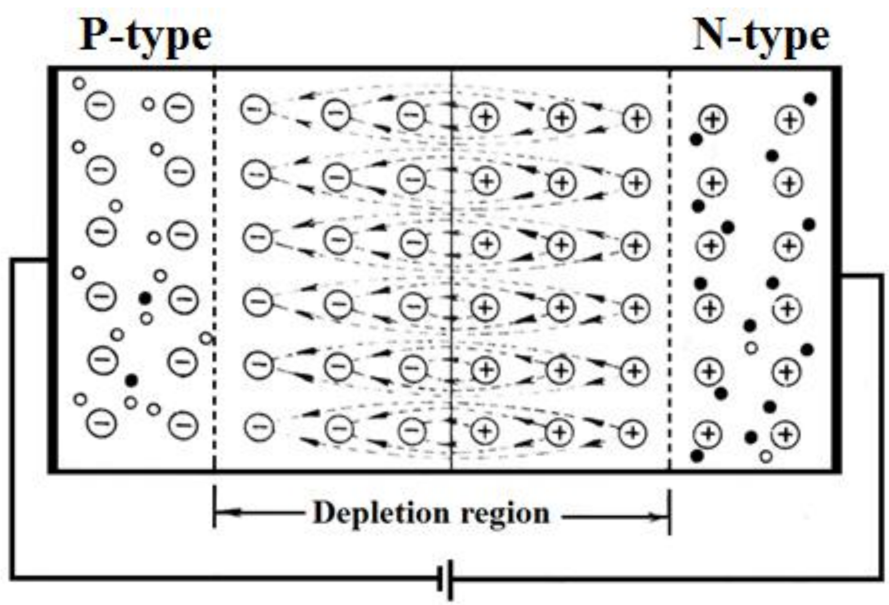




Space charge region or depletion region is formed in the vicinity of the junction. Barrier potential is about 0.7 V for Si and 0.3 V for Ge.



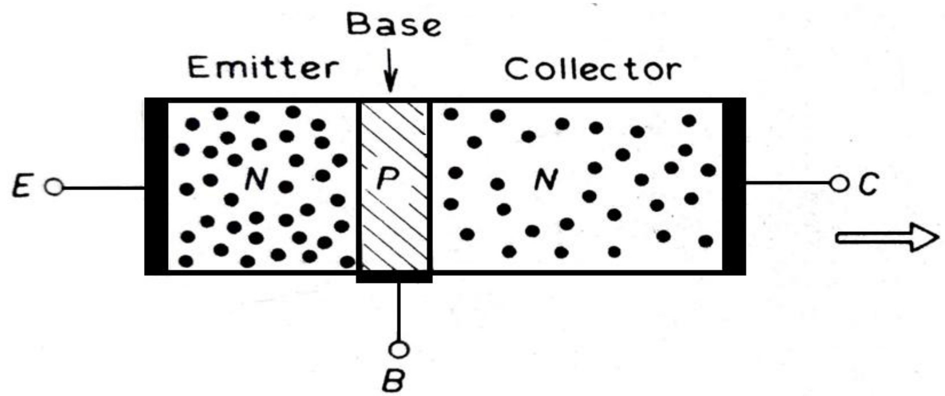
PN-junction showing forward bias



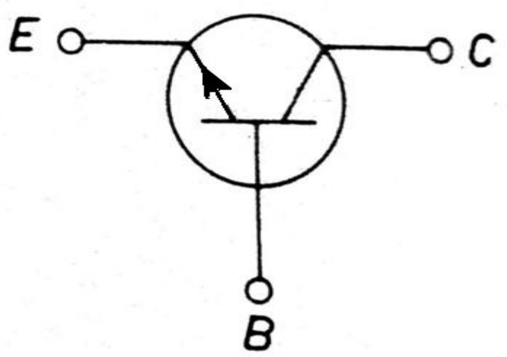
PN-junction showing reverse bias

Transistor- Consist of two PN-junctions formed by sandwiching either P-type or N-type semiconductor between a pair of opposite types.

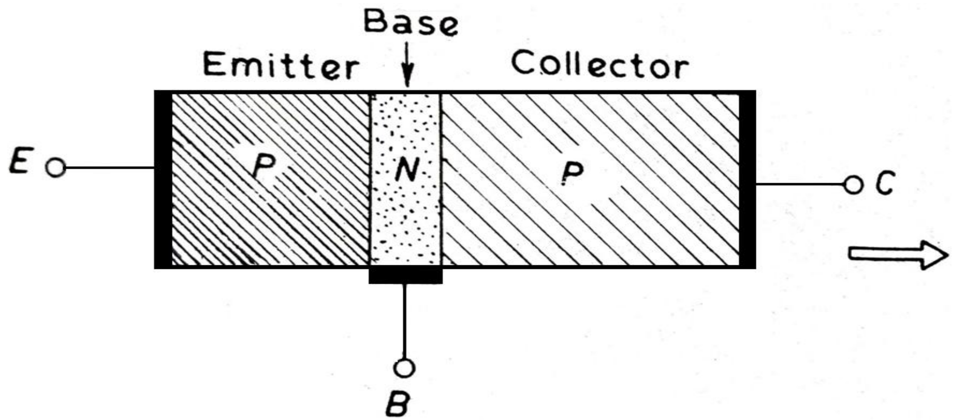
NPN -Transistor



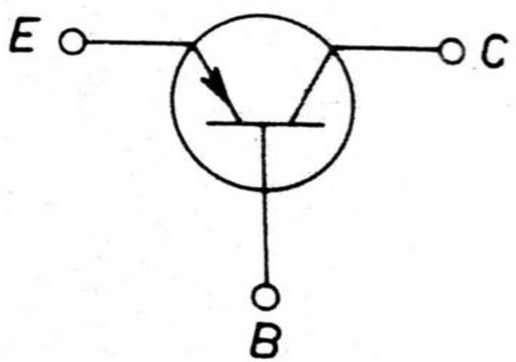
Symbol



PNP -Transistor



Symbol



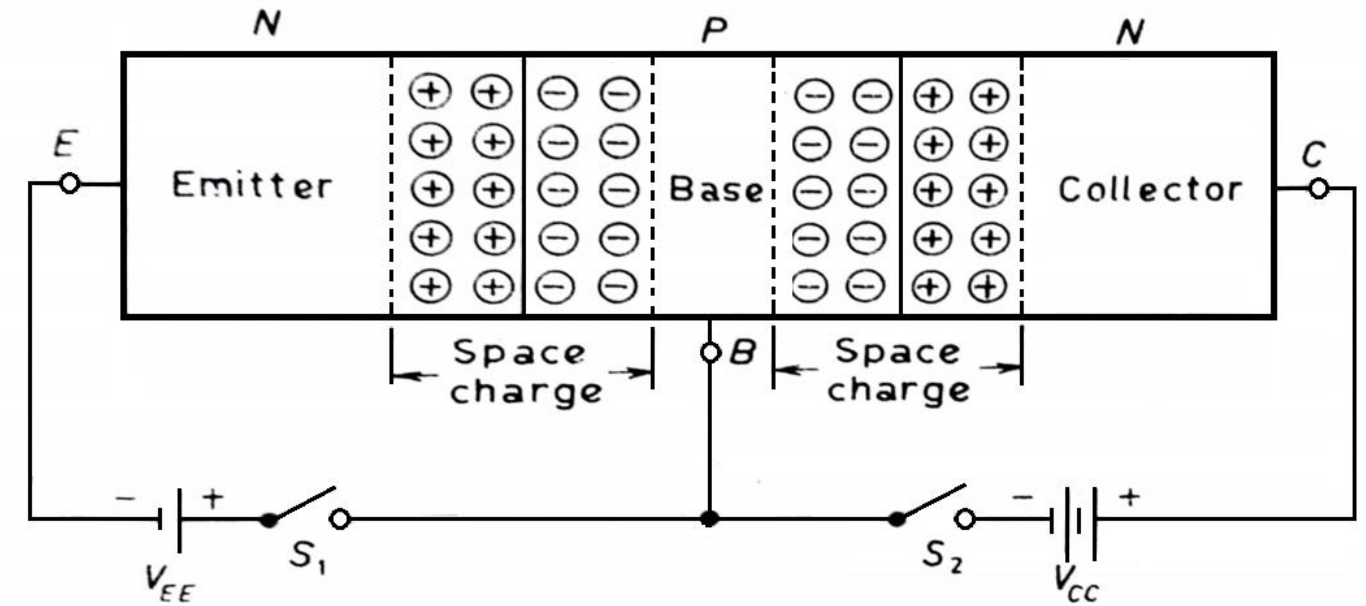
A transistor has two PN-junctions. One junction is between the emitter and the base (*emitter-base junction or simply emitter junction*). The other junction is between the base and the collector (*collector-base or simply collector junction*).

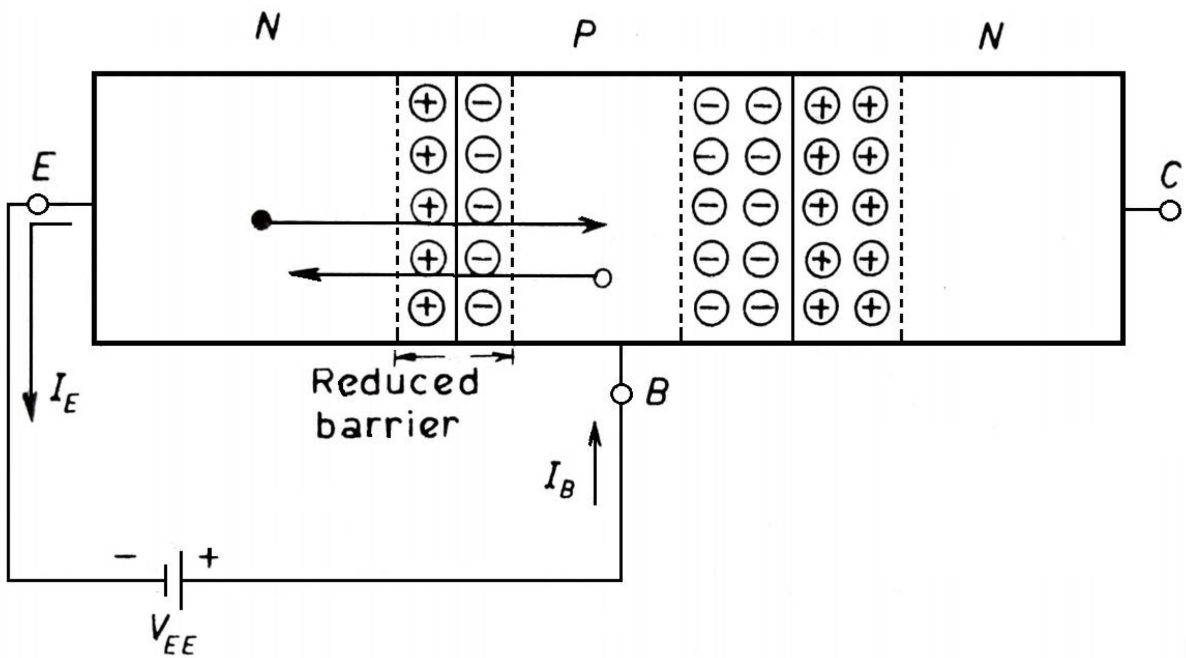
There are four possible ways of biasing these two junctions

Condition		Emitter junction	Collector junction	Region of operation
I	FR	Forward-biased	Reverse-biased	Active
II	FF	Forward-biased	Forward-biased	Saturation
III	RR	Reverse-biased	Reverse-biased	Cutoff
IV	RF	Reverse-biased	Forward-biased	Inverted

It is condition I (FR), where emitter junction is forward-biased and collector junction is reversed-biased, which is of our interest.

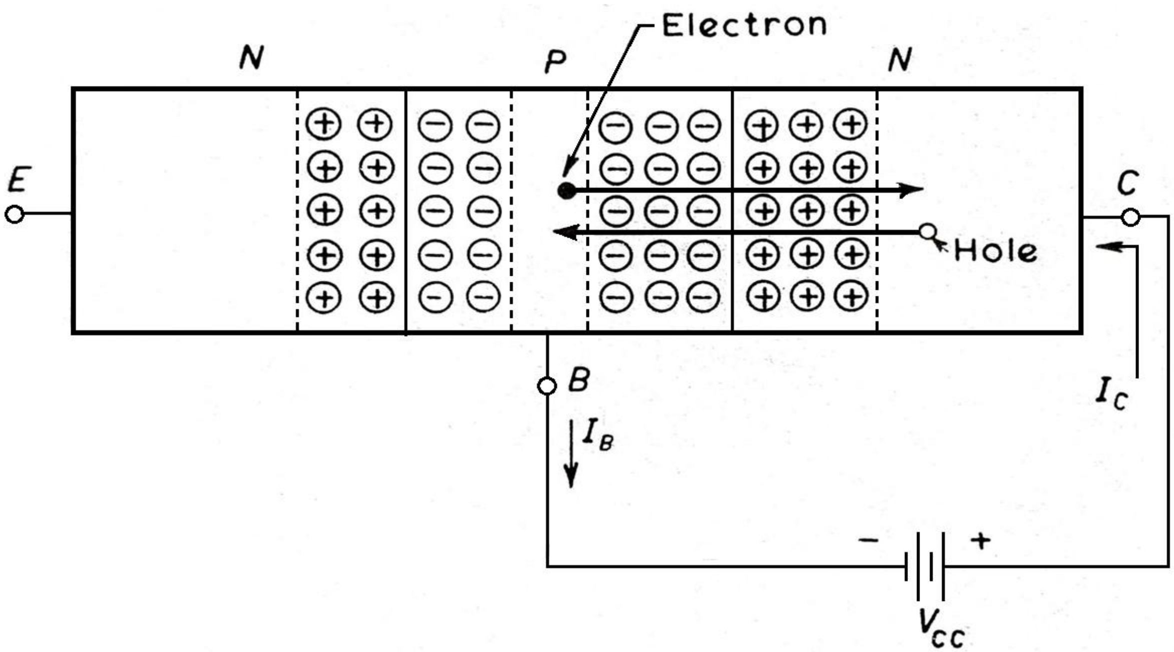
Biasing an NPN transistor for active operation:





Close the switch S_1 and keep switch S_2 open, the *emitter junction will be forward-biased-* ***a large current flows.*** 99% of the total current is carried by the electrons.

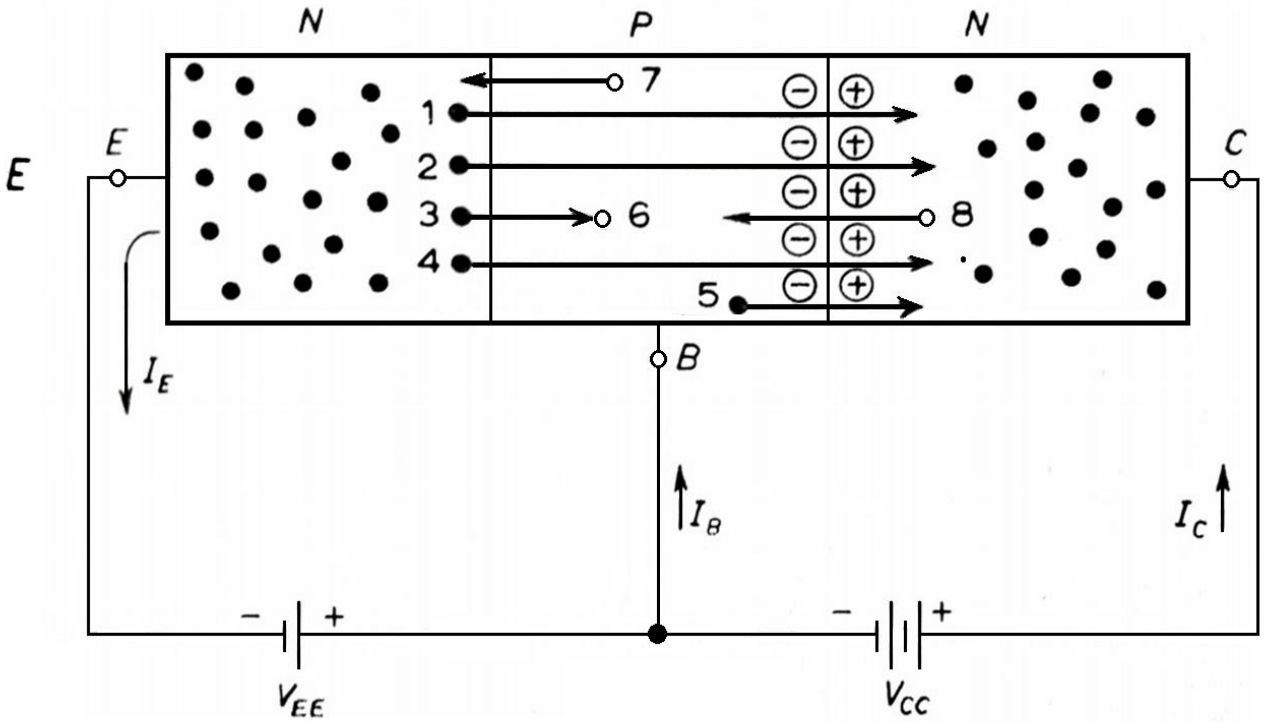
$I_E = I_B$ and $I_C = 0$



Next, we close the switch S_2 and keep the switch S_1 open, the *collector junction is reverse-biased-* *very small current flows. The reverse leakage current is due to the movement of minority carriers.* $I_C = I_B$ and $I_E = 0$

These carriers are accelerated by the potential barrier. This leakage current is very much temperature dependent. The small collector current is called the collector leakage current (I_{CBO}). The subscript CBO in this symbol signifies that it is a current between Collector and Base, when the third terminal (i.e., emitter) is Open.

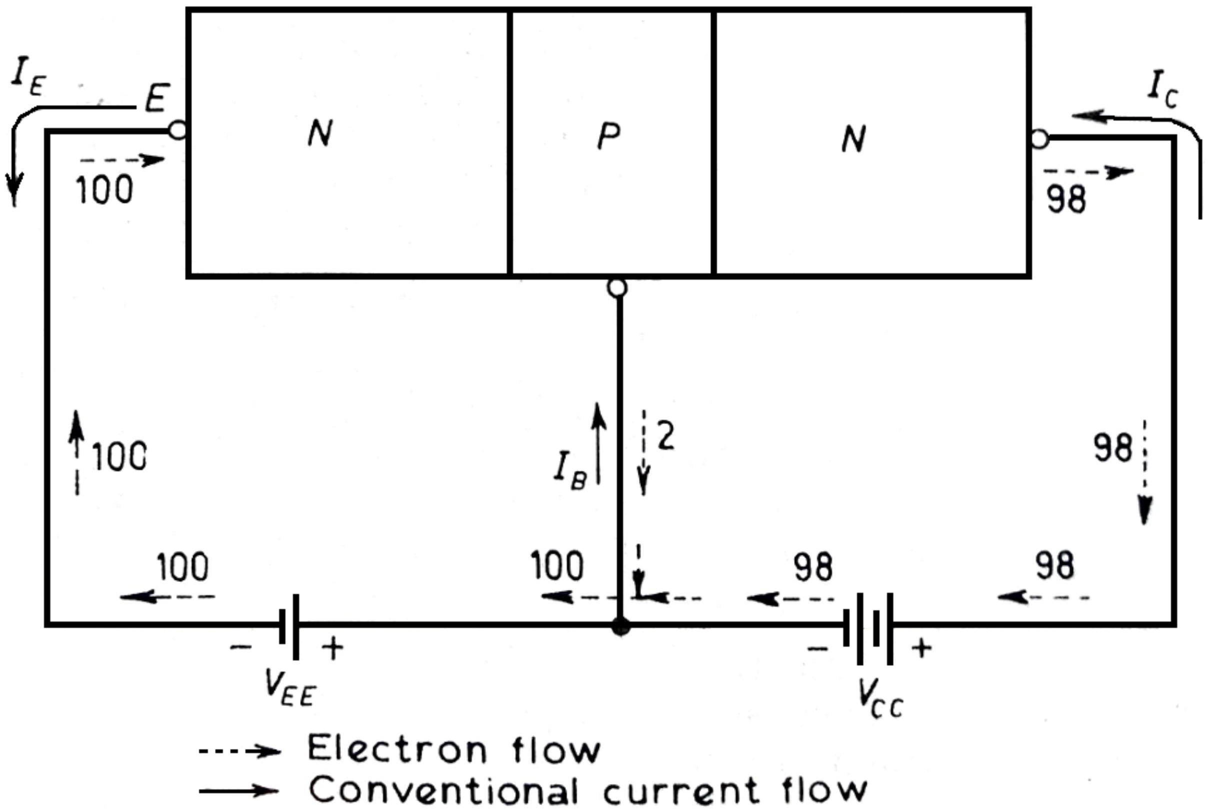
What should we expect if both switches S_1 and S_2 are closed?



- **The emitter current I_E is large, as expected, but I_B turns out to be very small current, and I_C turns out to be a large current.**
- **Electrons 1, 2, 3 and 4 crossing from emitter to base, and hole 7 from the base to the emitter, the total sum of these charge-carrier movements constitutes the emitter current I_E.**
- **Only a portion of this current is due to the movement of electrons 1, 2, 3 and 4. These are the electrons injected by the emitter into the base.**
- **The ratio of the electron current to the total emitter current is known as *emitter injection ratio*, or *the emitter efficiency* (γ), typically equals to 0.995.**

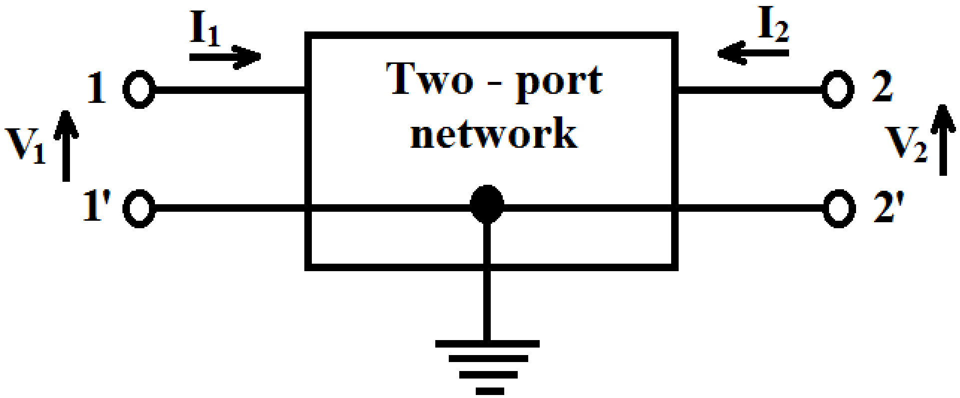
- **Since base is made very narrow and is very lightly doped, most of the minority carriers (electrons) travelling from the emitter end of the base region to its collector end do not recombine with holes in this journey.**
- **Only a few electrons (like 3) may recombine with holes (like 6). The ratio of the number of electrons arriving at collector to the number of emitted electrons is known as the *base transportation factor* (β'), typically equals to 0.995.**
- **Movement of hole 8, from the collector region and electron 5 from the base region constitute leakage current, I_{CBO}.**
- **Movement of electron 3 and hole 7 constitute a part of emitter current I_E. This current is not equal to I_{CBO}.**
- **Actually, the number of electrons (like 3) and hole (like 7) crossing the emitter base junction is much more than the number of electrons (like 5) and holes (like 8) crossing the collector-base junction. *The difference of these two currents in the base region makes the base current I_B*.**
- **I_C is less than the I_E. There are two reasons for this. Firstly, a part of the I_E consists of holes that do not contribute to the I_C. Secondly, not all the electrons injected into the base are successful in reaching the collector.**
- **The ratio of the I_C to the I_E is called dc *alpha* ($\alpha_{dc} = 0.99$) of the transistor.**

Relationship between different transistor currents

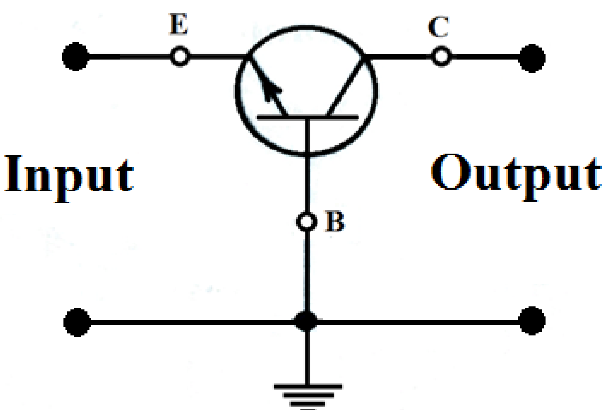


$$I_E = I_C + I_B$$

$$I_C = \alpha_{dc} I_E + I_{CO} \quad \text{where} \quad \alpha_{dc} = \frac{I_C}{I_E}$$

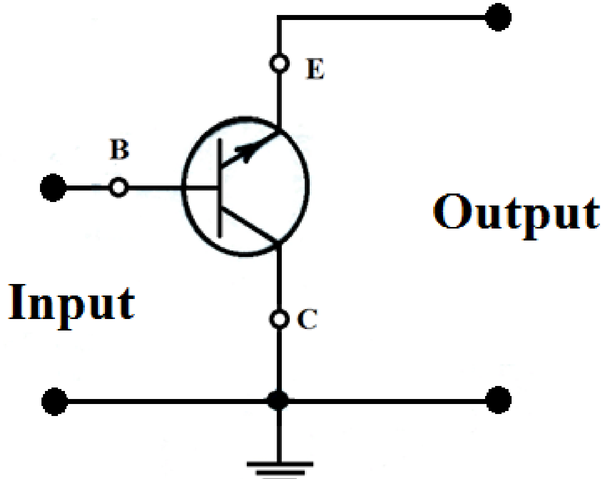


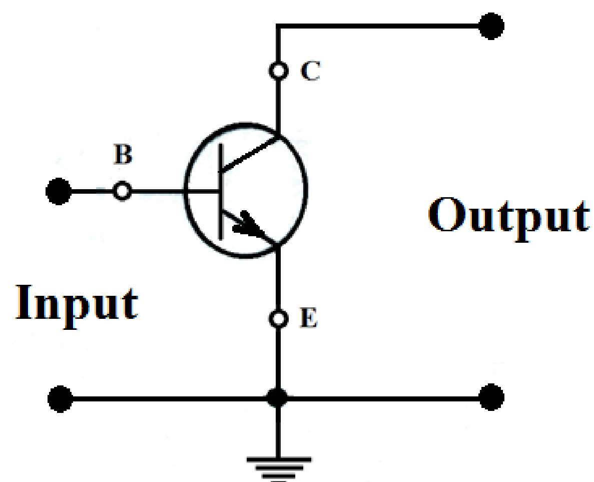
A transistor is a three terminal device. If one of the terminals is considered common to input and output, a transistor becomes a two-port device.



Common-Base (CB) configuration

Common-Collector (CC) configuration





Common-Emitter (CE) configuration

Objective: To draw characteristics of a PNP/NPN transistor in common base (CB) configuration and determine dynamic input resistance, dynamic output resistance and current gain.

Apparatus required: PNP transistor, batteries (1V & 10V), voltmeters (0-1V & 0-10V), ammeters (0-10 mA), rheostats.

Theory: (As explained earlier)

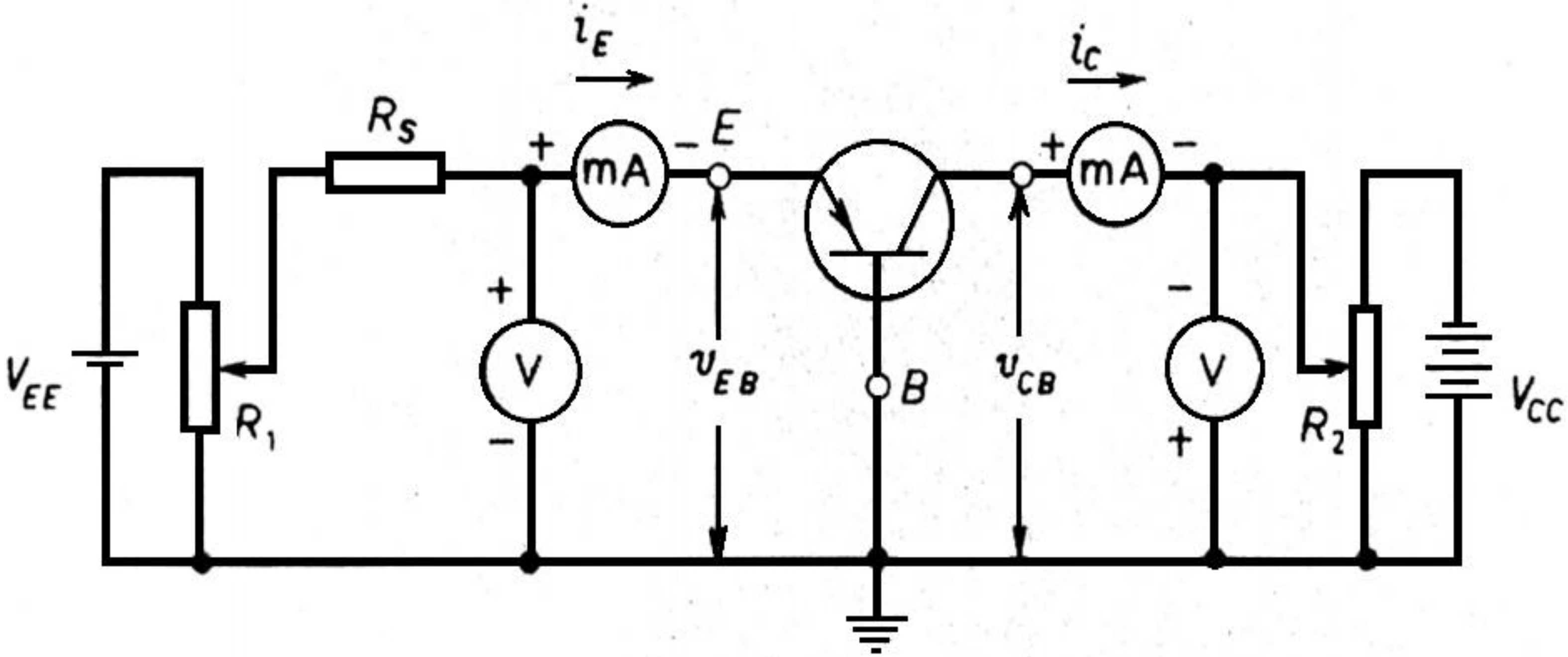
Input Characteristics: The common-base input characteristics are plotted between emitter current i_E and the emitter-base voltage v_{EB}, for different values of collector-base voltage v_{CB}.

Output Characteristics: The common-base output characteristics are plotted between collector current i_C and the collector-base voltage v_{CB}, with the emitter current i_E kept constant.

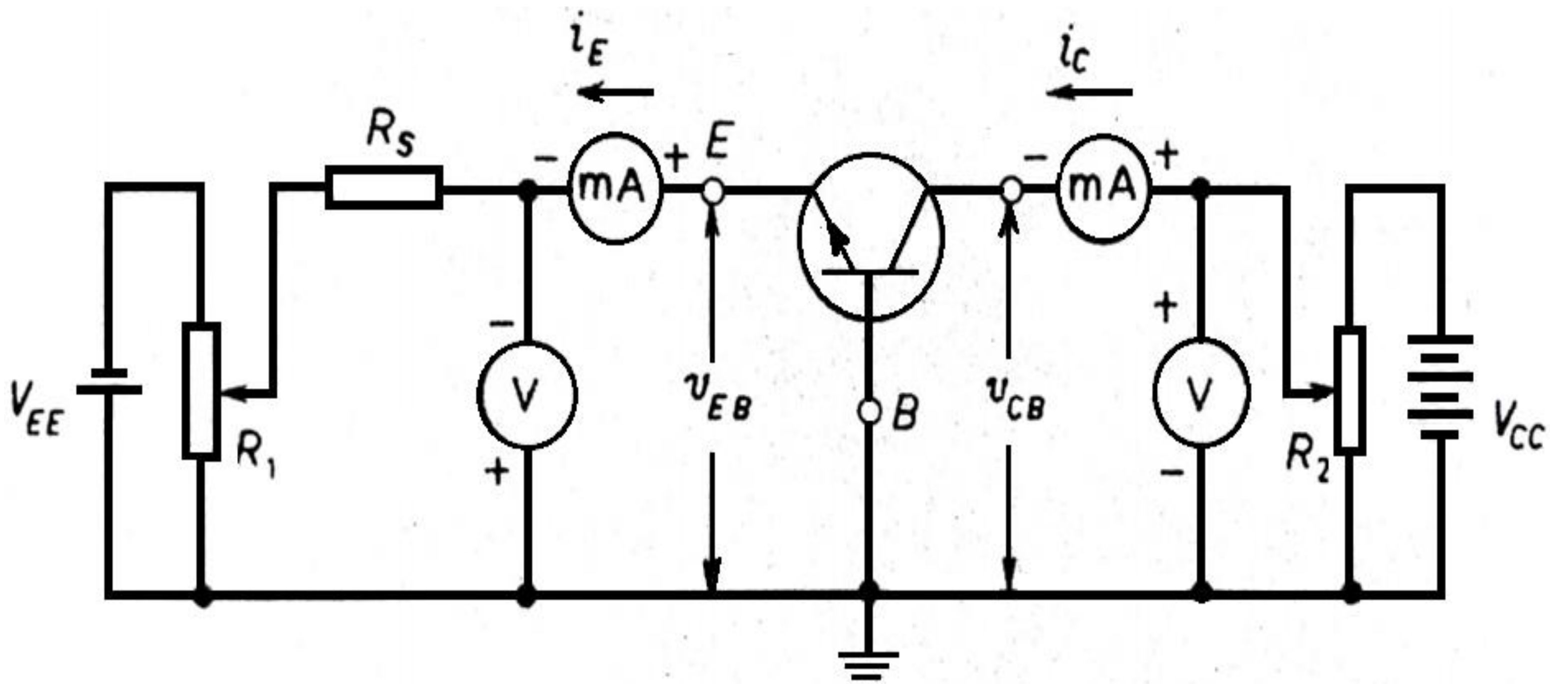
Dynamic input resistance : $$r_i = \left.\frac{\Delta v_{EB}}{\Delta i_E}\right|_{V_{CB}=\text{constant}}$$

Dynamic output resistance : $$r_o = \left.\frac{\Delta v_{CB}}{\Delta i_C}\right|_{I_E=\text{constant}}$$

DC current gain : $$\alpha_{dc} = \frac{I_C}{I_E}$$



Circuit diagram for PNP transistor



Circuit diagram for NPN transistor

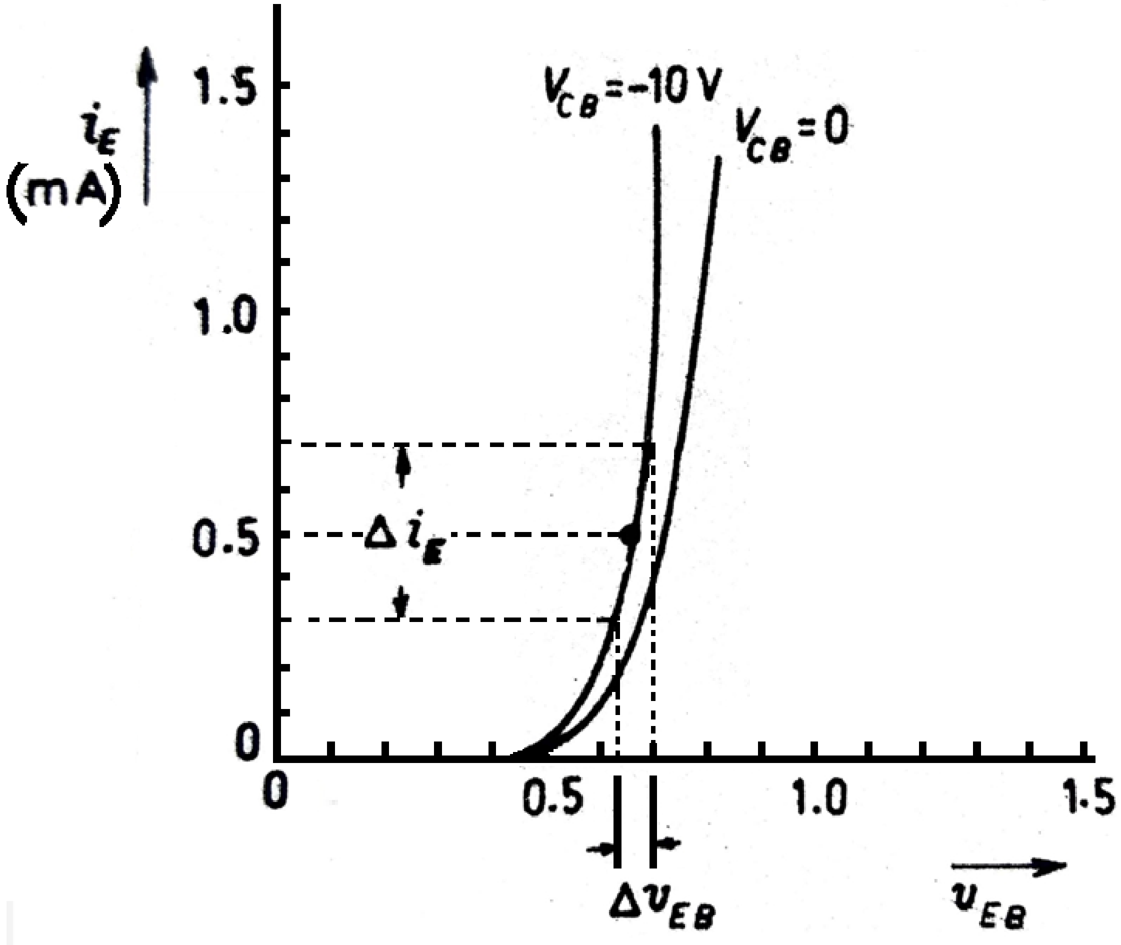
Observation table for input characteristics of PNP/NPN transistor:

S. No.	$V_{CB} = 0V$		$V_{CB} = -10V$	
	V_{EB}	I_E	V_{EB}	I_E
1				
2				
3				
4				
-				
-				

Observation table for output characteristics of PNP/NPN transistor:

S. No.	$I_E = 0.5$ mA		$I_E = 1$ mA		$I_E = 1.5$ mA	
	V_{CB}	I_C	V_{CB}	I_C	V_{CB}	I_C
1						
2						
3						
4						
-						
-						

Input characteristics of PNP transistor:



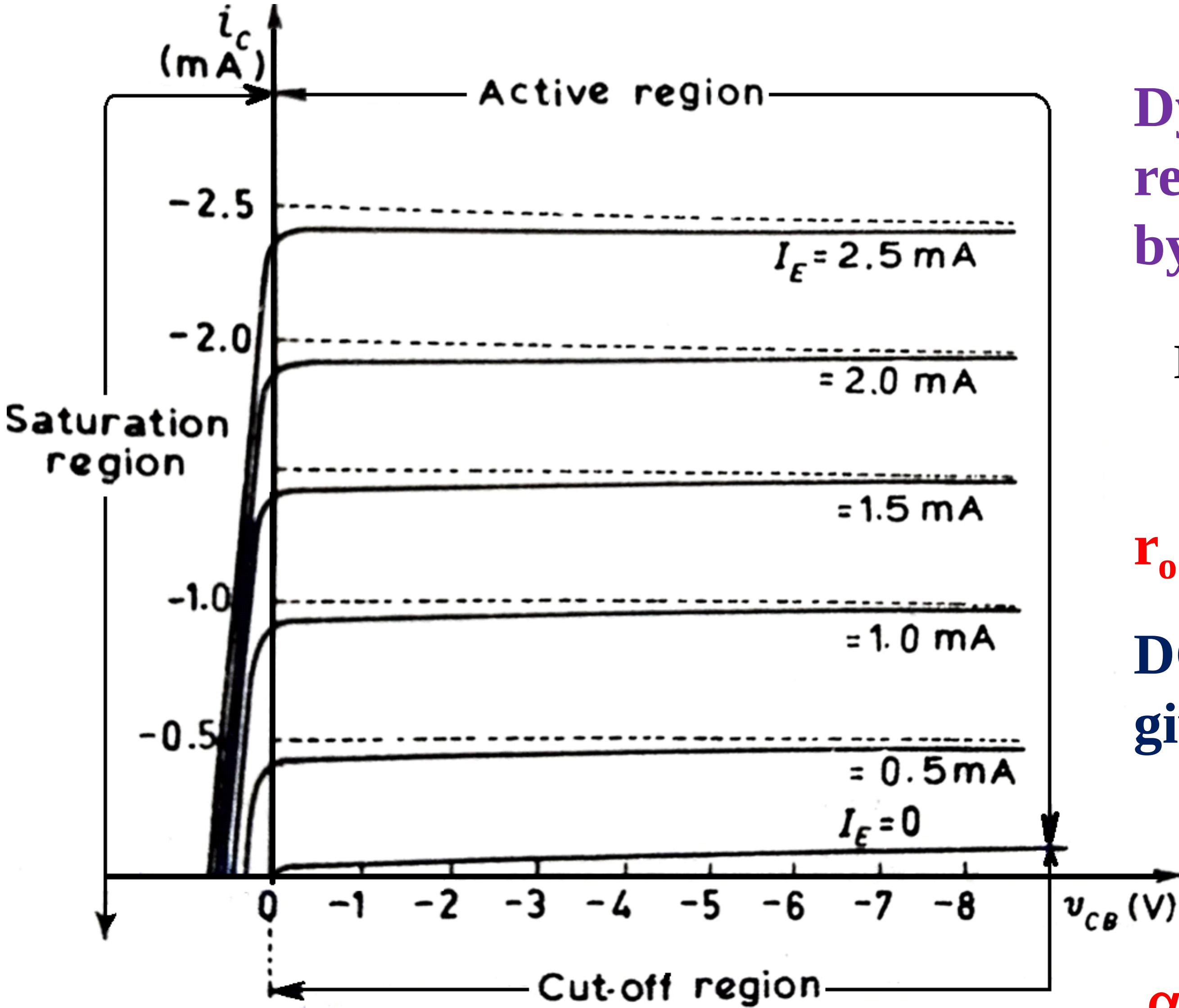
Dynamic input resistance is given by –

$$r_i = \left.\frac{\Delta v_{EB}}{\Delta i_E}\right|_{V_{CB}=\text{constant}}$$

r_i is very low (20 to 100Ω)

The input characteristics of NPN transistor are similar to those of PNP, differing only in that both i_E and v_{EB} would be negative and V_{CB} would be positive.

Output characteristics of PNP transistor:



Dynamic output resistance is given by –

$$r_o = \left.\frac{\Delta v_{CB}}{\Delta i_C}\right|_{I_E = \text{constant}}$$

r_o is very high (1 MΩ)

DC current gain is given by –

$$\alpha_{dc} = \frac{I_C}{I_E}$$

α = 0.98 (approx.)

Objective: **To draw characteristics of a PNP/NPN transistor in common emitter (CE) configuration and determine dynamic input resistance, dynamic output resistance and current gain.**

Apparatus required: **PNP transistor, batteries (1V & 10V), voltmeters (0-1V & 0-10V), ammeters (0-500 μA & 0-10mA), rheostats.**

Theory: (As explained earlier)

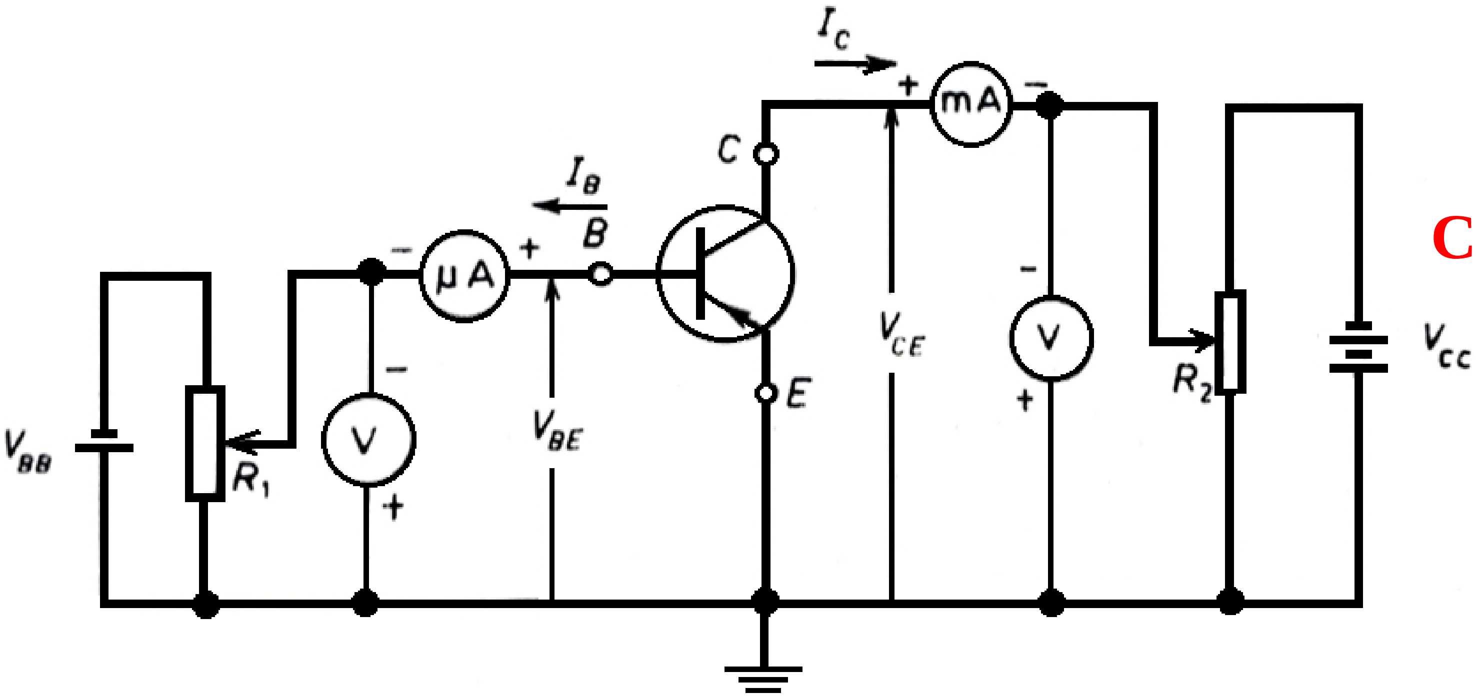
Input Characteristics: **The common-emitter input characteristics are plotted between base current i_B and the base-emitter voltage v_{BE}, for different values of collector-emitter voltage v_{CE}.**

Output Characteristics: **The common-emitter output characteristics are plotted between collector current i_C and the collector-emitter voltage v_{CE}, with the base current i_B kept constant.**

Dynamic input resistance : $$r_i = \left.\frac{\Delta v_{BE}}{\Delta i_B}\right|_{V_{CE}=\text{constant}}$$

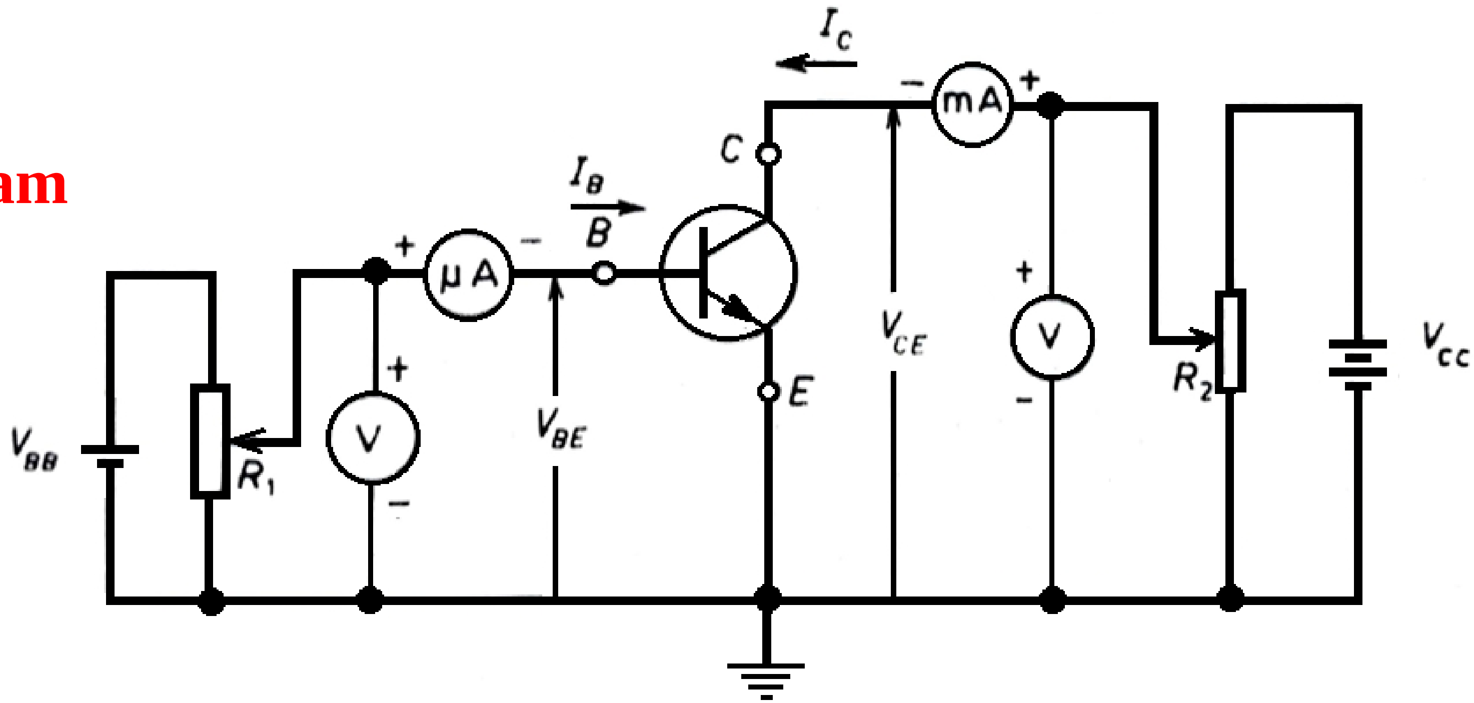
Dynamic output resistance : $$r_o = \left.\frac{\Delta v_{CE}}{\Delta i_C}\right|_{I_B=\text{constant}}$$

DC current gain : $$\beta_{dc} = \frac{I_C}{I_B}$$



Circuit diagram for PNP transistor

Circuit diagram for NPN transistor



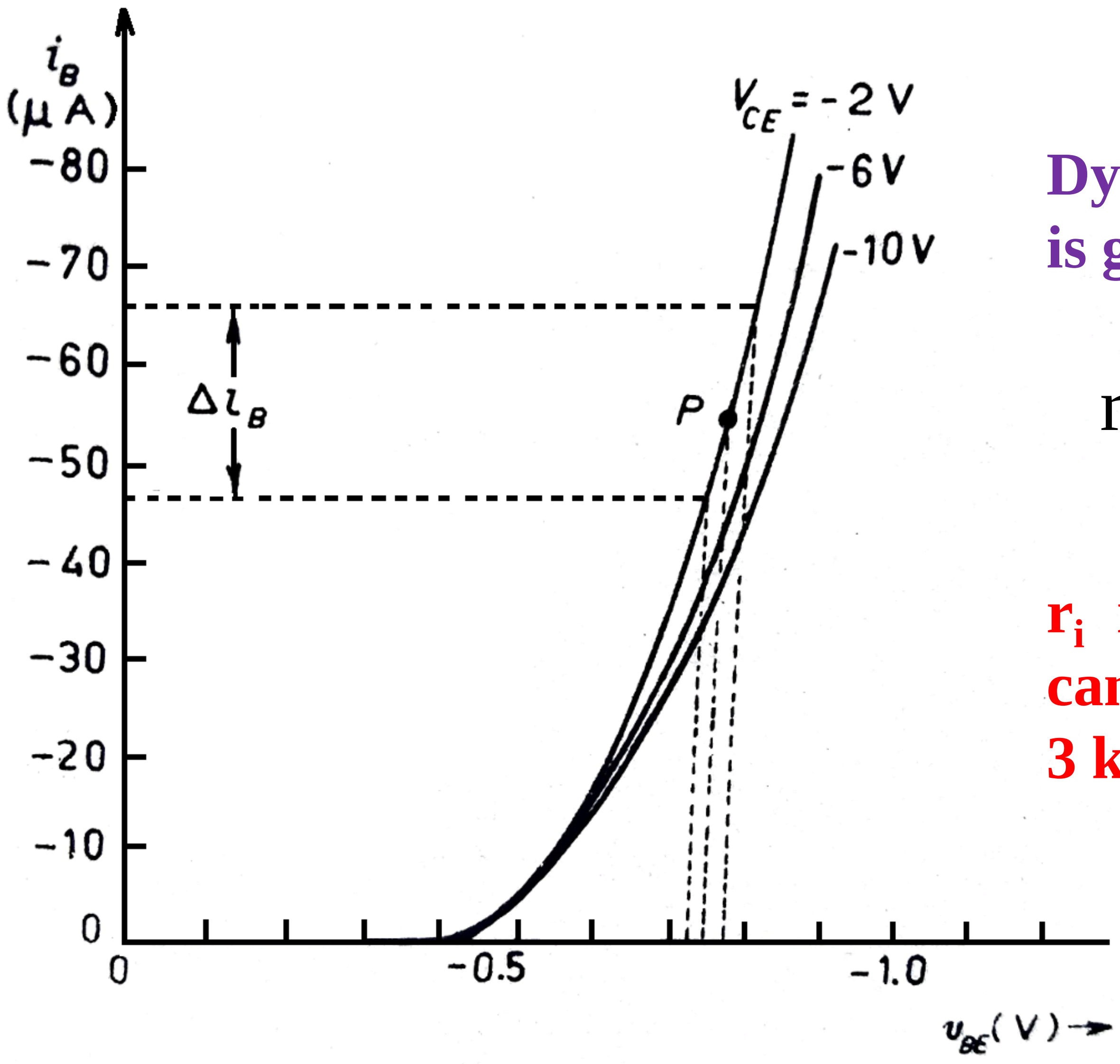
Observation table for input characteristics of PNP/NPN transistor:

S. No.	V_{CE} = -2V		V_{CE} = -6V		V_{CE} = -10V	
	V_{BE}	I_B	V_{BE}	I_B	V_{BE}	I_B
1						
2						
3						
4						
-						
-						

Observation table for output characteristics of PNP/NPN transistor:

S. No.	I_B = 10 μA		I_B = 20 μA		I_B = 30 μA	
	V_{CE}	I_C	V_{CE}	I_C	V_{CE}	I_C
1						
2						
3						
4						
-						
-						

Input characteristics of PNP transistor:

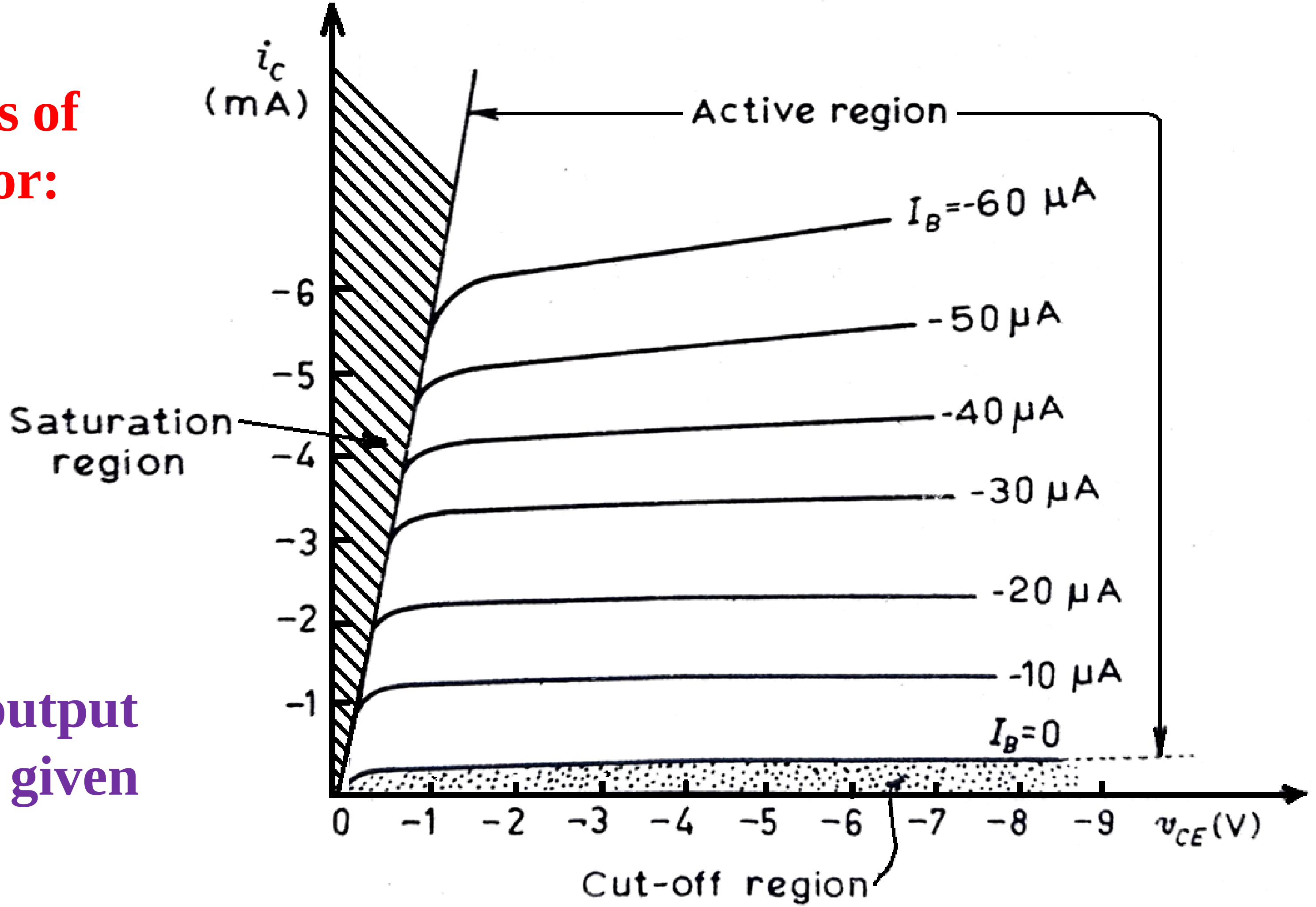


Dynamic input resistance is given by –

$$r_i = \left.\frac{\Delta v_{BE}}{\Delta i_B}\right|_{V_{CE}=\text{constant}}$$

r_i is typically 1 kΩ but can range from 800 Ω to 3 kΩ.

Output characteristics of PNP transistor:



Dynamic output resistance is given by –

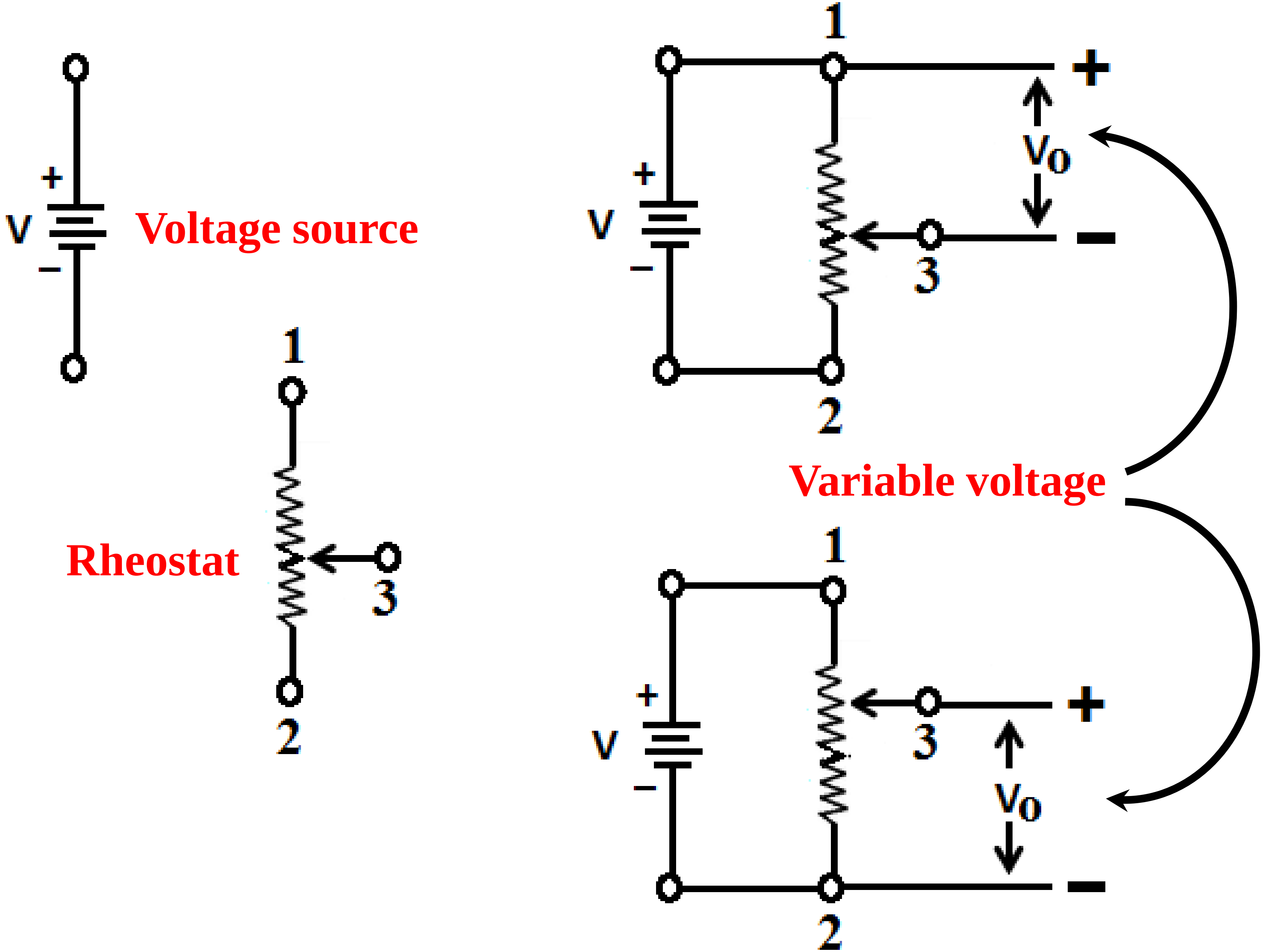
$$r_o = \left.\frac{\Delta v_{CE}}{\Delta i_C}\right|_{I_B = \text{constant}}$$

r_o is high (10 kΩ)

DC current gain is given by –

$$\beta_{dc} = \frac{I_C}{I_B}$$

β = 100 (approx.)



V
+
−
Voltage source
1
Rheostat
3
2
V
+
−
1
3
2
+
Vo
−
Variable voltage
V
+
−
1
3
2
+
Vo
−