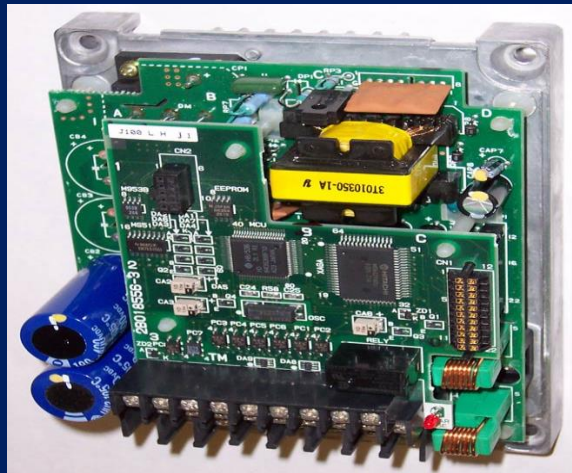
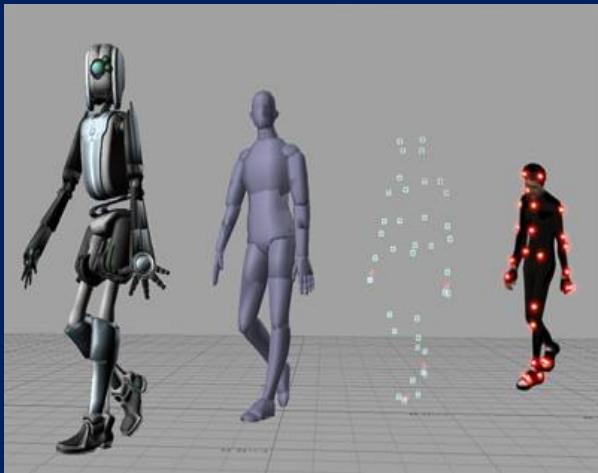




MSCPH-523(L)

M. Sc. III SEMESTER

Practical Physics III



**DEPARTMENT OF PHYSICS
SCHOOL OF SCIENCES
UTTARAKHAND OPEN UNIVERSITY**

Board of Studies

Prof. P. D. Pant

Director School of Sciences
Uttarakhand Open University, Haldwani

Prof. P. S. Bisht,

SSJ Campus, Kumaun University, Almora.

Dr. Kamal Devlal

Department of Physics
School of Sciences, Uttarakhand Open University

Prof. S.R. Jha,

School of Sciences, I.G.N.O.U.,
Maidan Garhi, New Delhi

Prof. R. C. Shrivastva,

Professor and Head, Department of
Physics, CBSH, G.B.P.U.A.&T.
Pantnagar, India

Pogramme Coordinator : Dr. Kamal Devlal

<h3>Department of Physics (School of Sciences)</h3>

<p>Dr. Kamal Devlal, Assistant Professor & Pogramme coordinator</p>
--

<p>Dr. Vishal Sharma, Assistant Professor</p>
--

<p>Dr. Gauri Negi, Assistant Professor</p>

<p>Dr. Meenakshi Rana, Assistant Professor (AC)</p>
--

<p>Dr. Rajesh Mathpal, Assistant Professor(AC)</p>

Unit writing and Editing

Editing**Dr. Rajesh Mathpal**

Department of Physics
School of Sciences, Uttarakhand Open
University

Writing**1. Dr. Kamal Devlal**

Department of Physics
School of Sciences, Uttarakhand Open University

2. Dr. Rajesh Mathpal

Department of Physics
School of Sciences, Uttarakhand Open University

3. Dr. Rajesh Mathpal

Department of Physics
School of Sciences, Uttarakhand Open University

<p>Course Title and Code : Practical Physics III MSCPH-523(L)</p>
--

<p>ISBN :</p>

<p>Copyright : Uttarakhand Open University</p>

<p>Edition : 2022</p>

<p>Published By : Uttarakhand Open University, Haldwani, Nainital- 263139</p>
--

<p>Printed By :</p>

MSCPH-523 (L)

Practical Physics III



**DEPARTMENT OF PHYSICS
SCHOOL OF SCIENCES
UTTARAKHAND OPEN UNIVERSITY**

Phone No. 05946-261122, 261123

Toll free No. 18001804025

Fax No. 05946-264232, E. mail info@uou.ac.in

<http://uou.ac.in>

Contents

Course 13: Practical Physics III

Course code: MSCPH523 (L)

Credit: 3

Unit number	Block and Unit title	Page number
Practical Physics III		
1	GM Counter	5-14
2	Flip Flop	15-24
3	Power Supply	25-28
4	Fiber Optics	29-43
5	Register	44-60
6	Decoder	61-75
7	Multiplexer and Demultiplexer	76-80
8	Comperator	81-93

EXPERIMENT NO. 1. BASIC IDEA ABOUT RADIOACTIVITY MEASUREMENT (GM COUNTER)

1.1 RADIATION

1.2 TYPES OF RADIATIONS

1.3 DETECTION AND MEASUREMENTS

1.4 GAS IONISATION DETECTORS

1.5 CHARACTERISTICS VOLTAGE CURRENT CURVE FOR IONISATION DETECTORS

1.6 GEIGER MULLER COUNTER

1.7. OBJECT

1.8. PROCEDURE

1.1 RADIATION:

A term used for the propagation of electromagnetic radiation (visible light, infrared, ultraviolet x ray etc.) but extended to include corpuscular radiations such as alpha particles, beta particles neutrons and electrons.

1.2 TYPES OF RADIATIONS:

Radiations can be classified in two categories based on their ionisation behaviour of matter

(1) Ionising radiation: alpha particles, beta particles, positrons, X rays, heavy recoiling nuclei, protons etc. and electrons.

(2) Non ionising radiation: light photons, gamma rays, neutrons etc.

1.3 DETECTION AND MEASUREMENTS:

Instruments for the detection and measurement of radiation have basically two components a sensor element, and an indicating or reading element (recorder). Depending on the property of radiation the sensor is to be selected. Following are the some types of detectors.

(i) Gas Ionisation Detectors: Ionisation chamber, proportional counters and GM counters.

(ii) Scintillation counters: (a) Solid crystal scintillation counter: NaI(Tl) and Anthracene
(b) Liquid scintillation counters

(iii) Photographic Emulsions: Films for radioautography

(iv) Solid state Dosimeters: Semiconductors, thermo-luminescent phosphors, Glass dosimeters

(v) Nuclear track detectors: Mica or artificial foils for detection of heavy particles.

The selection of detector depends on a numbers of factors. But the basic requirement is that a detector can easily absorb beta particles or high penetrating gamma rays. In this time we will focus on gas ionisation detectors especially on Ionisation chamber, proportional counters and GM counters.

1.4 GAS IONISATION DETECTORS:

This radiation detection instruments are based on collection and indication of ions formed by radiation in a gas filled in the device. Gas ionisation detectors are generally of cylindrical shape with a central rod (wire) which acts as an anode and the outer metallic sheath works as cathode. The cylinder (tube) is filled with suitable gas (ionizing gas). Thus cathode and anode are

separated by suitable ionizing gas. One open end of the cylinder is sealed by very thin metal coated mica film which acts as window of the incoming radiation as shown in figure 1.

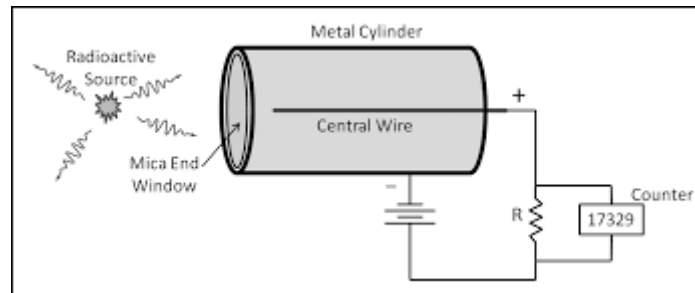


Figure 1.1: Gas ionisation detector

1.5 CHARACTERISTICS VOLTAGE CURRENT CURVE FOR IONISATION DETECTORS:

When a radioactive source is placed under the gas ionisation detector and a variable voltage is applied to the anode with respect to cathode, ionisation of filled gas takes place. Due to ionisation ion pairs are produced inside the detector and the positive and negative ions start move towards cathode and anode under the influence of electric voltage. If a graph is plotted between the applied voltages and corresponding current (which shows the number of ion pairs collected), the characteristic curve is obtained. The curve is shown in figure 2 with different regions.

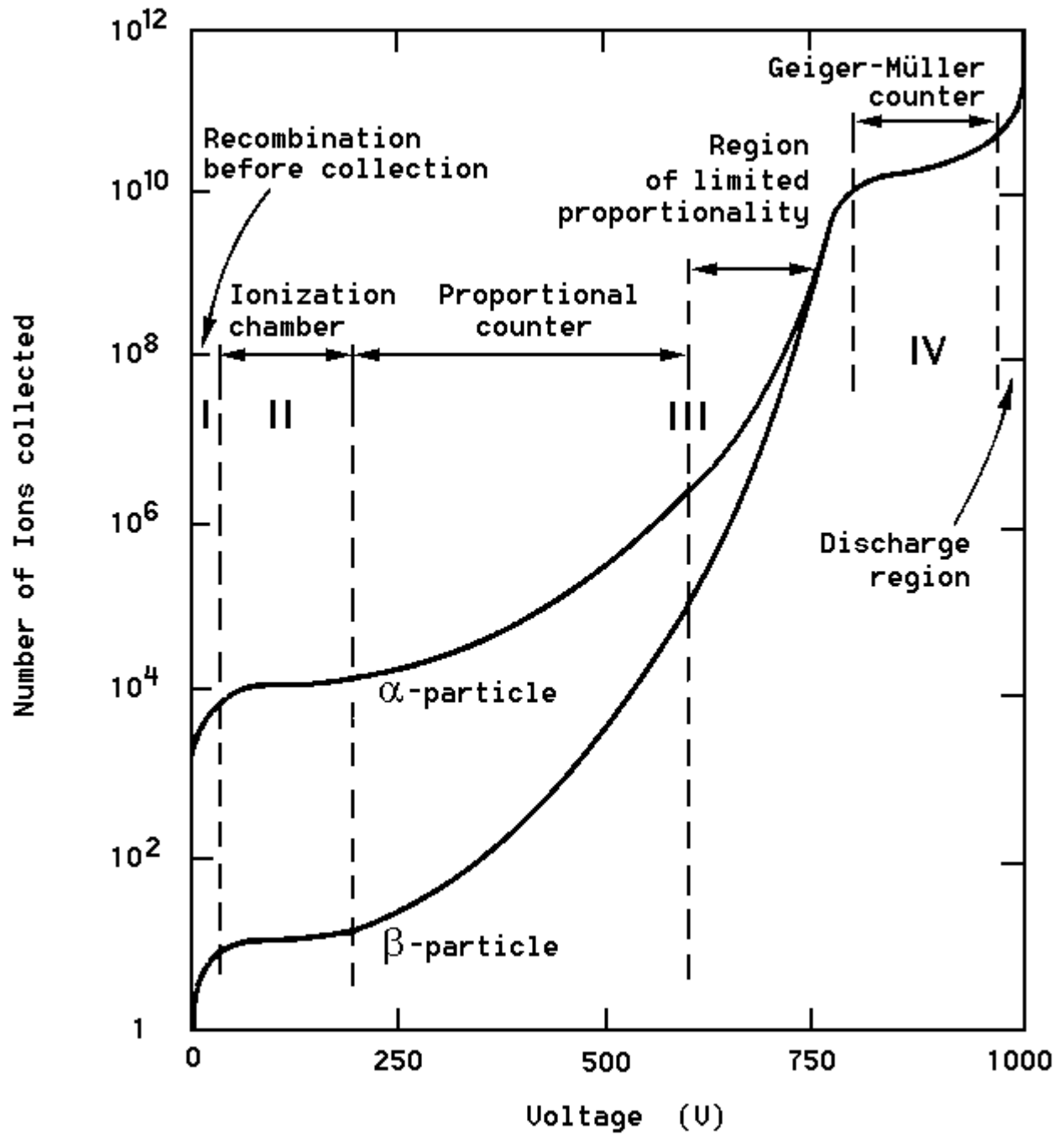


Figure 1.2: Characteristics voltage current curve for ionisation detectors

(1)Region of recombination: In this region applied voltage is low, and ion pairs are formed but some ion pairs recombine to form neutral atoms. The recombination decrease as applied voltage increases.

(2) Ionisation region: In this region, all the ion pairs are collected at cathode or anodes as there would be no recombination. The number of ion pairs produced and collected depends on the energy given by the radiation to the gas inside the detector.

(3) Region of proportionality: The negative ions or electrons in their path, towards the central electrode are accelerated because of electric field. The electrons gain sufficient energy to produce secondary ionisation, when they interact with ionised gas molecule. This results an increase in the number of ion pairs which is proportional to the energy dissipated by the incident radiation inside the sensitive volume of gas inside the detector. In this region the constant of proportionality increase with the increase in applied voltage and may be as high as 10^4 . In this region one can distinguish radiations of different energy and different types.

(4) Region of limited proportionality: In this region the amplification is not constant and it depends on the energy dissipation by incident radiation. This region is not generally used for counting.

(5) Geiger Muller (GM) region: This sensitive region spread over the entire length of the chamber and there will be no difference in the pulse height for the particles of different energies. In this region, gas amplification factor is very high therefore pulse height would be greater compared to that of ionisation chamber and proportional region. The gas amplification factor may be as high as 10^8 in this region.

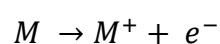
(6) Region of continuous discharge: In this region the voltages be higher than that for GM region, the positive ion start to bombard the cathode as a result UV radiation and electrons are emitted from the cathode which causes further ionisation. A continuous discharge and sparking takes place in this region. This region is not useful for the radiation detection.

The Ionisation region, proportionality region and GM region are commonly used for the radiation detector.

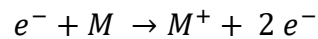
1.6 GEIGER MULLER COUNTER:

The GM detector has been the most widely used detector of nuclear radiation. It has high efficiency and used for the detection of different types of radiations, large size of output signal wide variety of shapes and comparatively low cost. The GM detector functions in GM region of ionisation curve, if any radiation particle enters in the GM detector, a discharge is produced i.e. an avalanche of ion pairs produce. The mechanism of discharge in GM counter can be as follows.

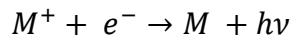
Step 1: Production of an ion pair in the counting chamber.



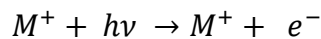
Step 2: Transport of ions towards electrodes. In the neighbourhood of the anode, the electrons become so accelerated that an amplification factor of 10^8 is reached through collision ionisation.



Step 3: Partial recombination of ions and electrons occurs to give highly excited gas molecules which emits photons.

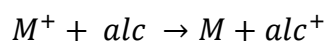


Step 4: Production of new ion pairs takes place in the gas space or at the cathode.



Through this process a charge avalanche is built up. Since the electron moves faster in the electric field than the positive ions, the positive charge cloud around the anode is reduced to such an extent that the collision ionisation stop until sufficient positive ions have migrated to the cathode. This time period is known as dead time during this period the detector is insensitive to primary ionisation. The dead time of GM counter is order of 10^{-4} sec. Under these conditions the pulses are recorded again when the potential of the anode wire is reaches its original value. Subsequently generation of secondary electrons continue through discharge of positive ions at the cathode. If this is not prevented by quenching, continue discharge would occur.

There are two types of GM counters; (a) unquenching type and (b) quenching type. In the unquenching detectors the continuous discharge is stopped by mean of high external resistance or by reversing the polarity of the applied potential. Whole the working with quenching detectors the continuous discharge is stopped due to the presence of alcohol (or methanol at 10 torr or bromine at 1 torr) in the filled gas say argon. Quenching is based on the transfer of positive charge through collision with the quenching agent.



The positive charge molecule of quenching agent dissociated on the way to cathode to yield fragments which cannot release secondary electrons.

To determine the dead time of GM counter the two source method is often used. Two radioactive sources of same activity are measures separately and together and the dead time can be calculated from the count rate I_1 , I_2 and $I_{1,2}$ by mean of relationship.

$$\frac{I_1}{1 - I_1 t} + \frac{I_2}{1 - I_2 t} = \frac{I_{1,2}}{1 - I_{1,2} t}$$

The figure 3 shows the complete experimental set up for the experiment. The tube is mounted on a structure which have different slots to place the source. The tube is connected to the GM Counter

Console which hosts the electronics for amplification and counting. It also provides the necessary power.



Figure 3: Experimental set up for GM Counter based experiments. Taken from the company manual <http://www.spectrumtechniques.com/resources/instrument-manuals/>

1.7. OBJECT: To study of characteristic curve of GM counter.

Purpose: The purpose of this experiment is to determine Plateau Characteristics of GM tube and to determine reasonable operating point for the tube.

Underlying Physical Aspects

We have now understood the basic working of GM tube. So, in order to observe the effect of incident radiation on GM tube, we need to increase the voltage between anode and cathode, to a value where the gas amplification sets in. This voltage is called the *Threshold Voltage* or *starting voltage*. Thereafter, the counting rate keeps on increasing till the voltage reaches a *knee value* beyond which the count rate becomes saturated or constant. In this constant region of operation all the primary events are recorded irrespective of the energy. This flat region is called *Plateau of the counter*. If we keep still keep on increasing the voltage, the tube will run in to continuous discharge region which is not desirable. The mid point of the plateau region is taken to be the *Operating Voltage* of the GM tube and once determined, the tube must be operated at this value for subsequent experiments.

1.8. PROCEDURE:

1. After setting up the GM tube and electronics we can start our experiment. Place the source at a distance of around 6 mm. One can set up a starting voltage say around 650 V with a step voltage of say 20 V. Set the preset time of 30 s.

2. Initially no counts will be registered. Around 750 V, there will be sudden increase in the counts, which would saturate around 800V. Though a small increase in counts will be registered through the experiment.
3. Stop the experiment at around 1200 V or before.
4. As we know that there are background counts in the laboratory. So, whatever counts we have registered, have to be corrected for background counts. One can repeat the steps 1-3, without a source. The process should be repeated twice or thrice and average of the same should be taken to be the background at each voltage. Make sure that no source lies nearby otherwise that might contribute to the background count.
5. Subtract the corresponding background count from each reading and register the correct counts vs voltage in table1.
6. A demo labeled plot of Counts vs Voltage is shown in Fig.4. You should plot Corrected Count Rate vs Voltage.

Inference

- Starting Voltage ± [We have least measuring voltage value of 1 V. What error should we mention in the result : either the instrumental value or the graphical one ?]

Table 1: Data Table for GM Plateau

S. No.	Voltage (V)	Counts	Avg. Bkg. Counts	Corrected Counts	Corrected Count rate
1.	650				
2.	670				
3.					
4.					
5.					
6.					

- Knee Voltage ±.....
- Range of Plateau ±..... [While calculating error, keep in consideration that the range is calculated as the difference of two voltage values.]
- Operating Voltage ±.....
- $$\text{Percentage slope of Plateau} = \frac{\text{Slope of the plateau region}}{\text{Knee Voltage * Voltage Difference of Plateau region}} * 100$$

Post Lab Questions and Take Home Messages

1. Will the operating voltage remain same if the present tube is replaced by another one ?
2. Will this operating voltage remain constant even after long period of time, say, ten years ?
3. What does the slope of plateau shows ? Why do we have slope, however small it may be ?

4. What will happen if we place the source at the last groove ? We might get the answer in subsequent experiments.
5. For background, we have taken two or three different readings at each voltage and every time we found that we did not get the same reading as previous one. But, the reading varies about certain value. Will it be the same for counts with the sources? You can check yourself by repeating the counting at operating voltage. And if it varies like the background count, then the data which we have acquired is not correct. What is the remedy to this problem? Again upcoming experiments may help us to get the answer to our question.

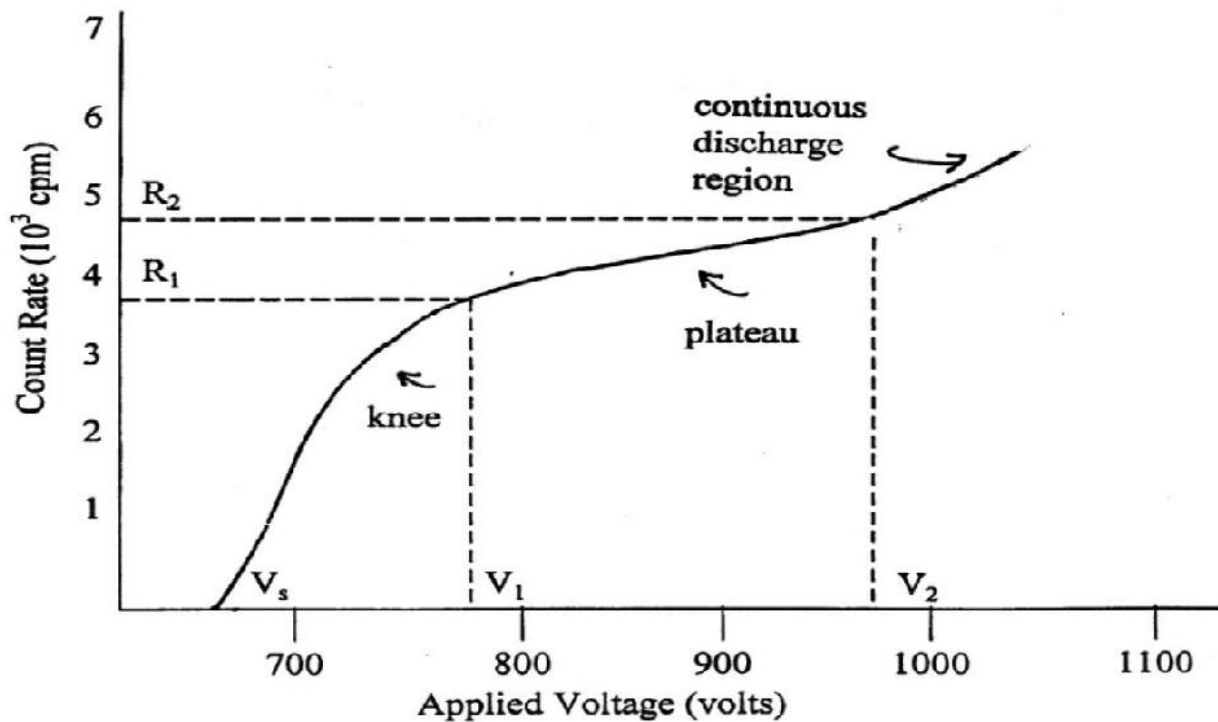


Figure 4: characteristic curve of GM counter

EXPERIMENT-2 : STUDY OF FLIP FLOP

2.1. OBJECTIVE

2.2. APPARATUS

2.3. INTRODUCTION

2.4. PROCEDURE

2.5. OBSERVATIONS

2.6. RESULTS

2.7. VIVA VOCE

2.1. OBJECTIVE: Verify the truth table of RS, JK, T and D flip-flops using NAND & NOR gates.

2.2. APPARATUS: Flip flop box, connecting wires.

2.3. INTRODUCTION: In electric circuit any device or circuit has two stable states called Bistable states. For example toggle switch has bistable states. Switch can be considered as memory device as it will remain as set until someone changes its position. A flip-flop (or latch) is a circuit that has two stable states. For example its output may be 0 or 1 (0 or +5V). The flip-flop also has memory since its output will remain as it is set until someone changes it, and can be used as a memory device. Flip-flops are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs.

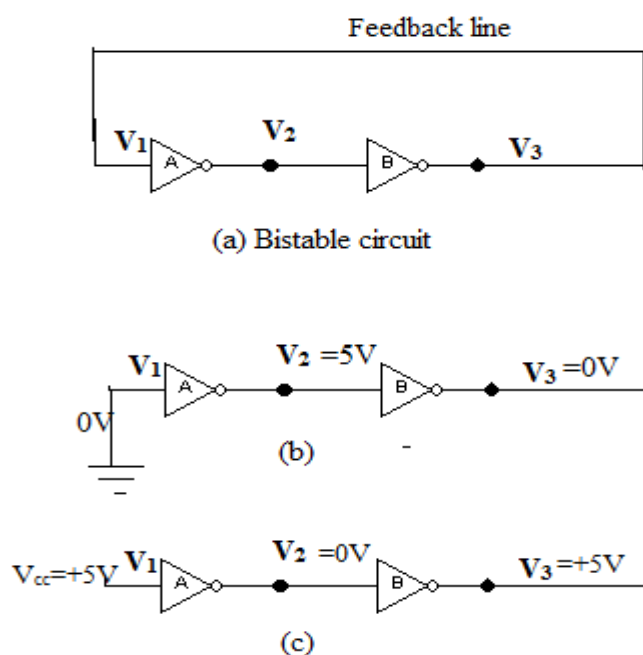


Figure 2.1: Basic Flip Flop

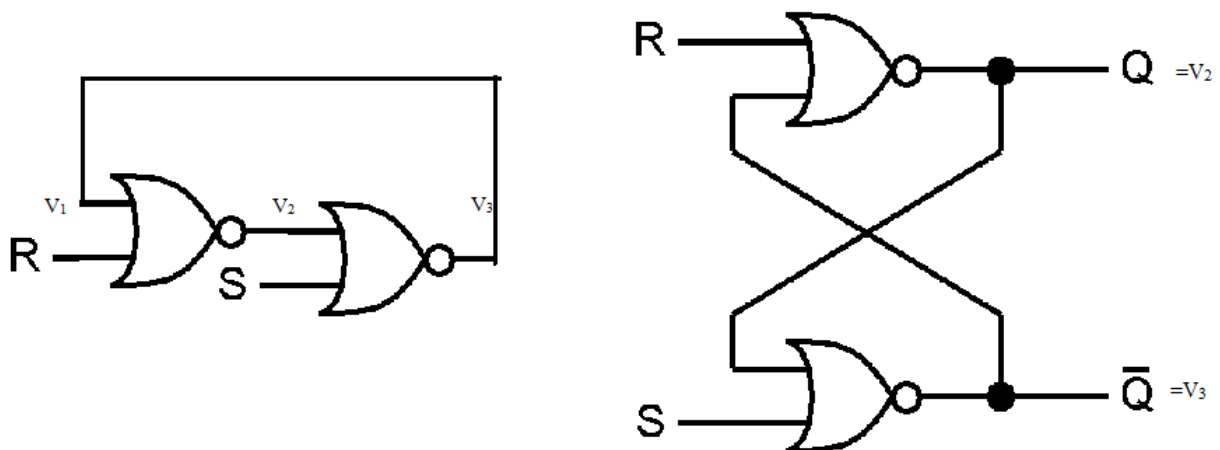


Figure 2: NOR gate Flip Flop

A flip flop is an electronic circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying inputs. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

- 1) R-S flip flop
- 2) D flip flop
- 3) J-K flip flop
- 4) T flip flop

1) R-S flip flop: The basic NAND gate RS flip flop circuit is used to store the data and thus provides feedback from both of its outputs again back to its inputs. The RS flip flop actually has three inputs, SET, RESET and its current output Q relating to its current state as shown in figure below.

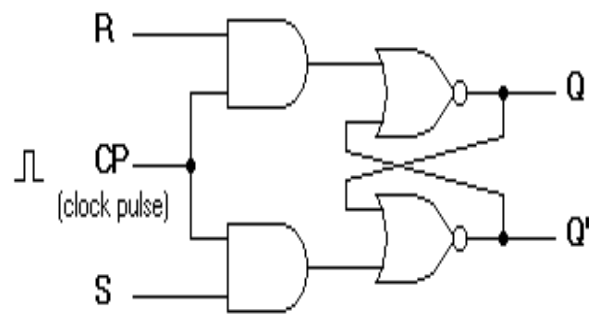


Figure 2.3

2) D flip flop:

A D flip flop has a single data input. This type of flip flop is obtained from the SR flip flop by connecting the R input through an inverter, and the S input is connected directly to data input. The modified clocked SR flip-flop is known as D-flip-flop and is shown below. From the truth table of SR flip-flop we see that the output of the SR flip-flop is in unpredictable state when the inputs are same and high. In many practical applications, these input conditions are not required. These input conditions can be avoided by making them complement of each other.

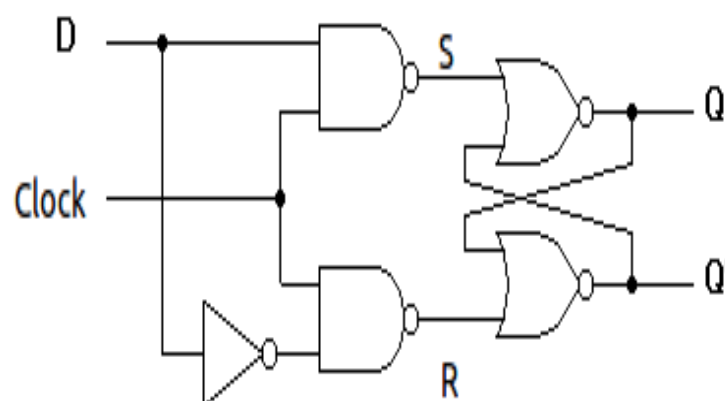


Figure 2.4

3) J-K flip flop: In a RS flip-flop the input $R=S=1$ leads to an indeterminate output. The RS flip-flop circuit may be re-joined if both inputs are 1 than also the outputs are complement of each other as shown in characteristics table below.

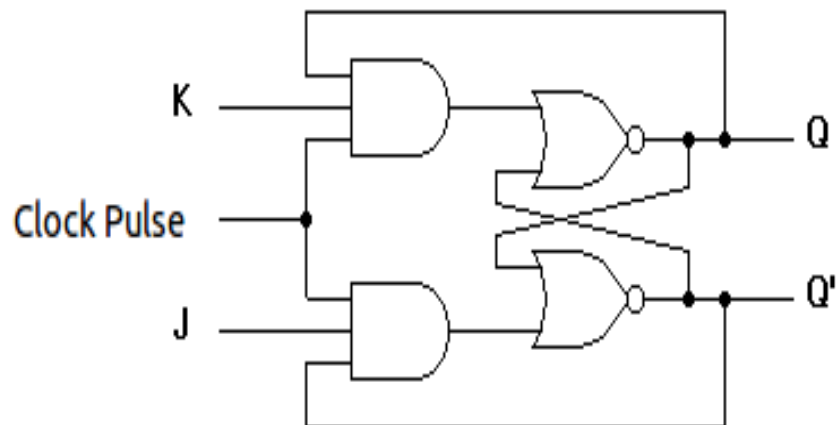


Figure-2.5: Circuit diagram of J-K flip flop

4) T flip flop:

T flip-flop is known as toggle flip-flop. The T flip-flop is modification of the J-K flip-flop. Both the JK inputs of the JK flip – flop are held at logic 1 and the clock signal continuous to change as shown in table below.

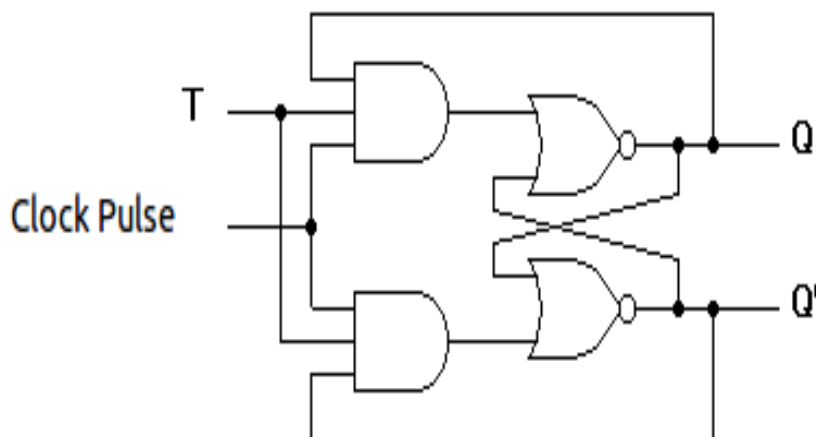


Figure2.6: Circuit diagram of T flip flop

2.4. PROCEDURE:

1) RS flip flop

Step-1: Connect the supply (+5V) to the circuit.

Step-2: First press "ADD" button to add basic state of your output in the given table.

Step-3: Press the switches to select the required inputs "S" and "R" and apply the clock pulse.

Step-4: Press "ADD" button to add your inputs and outputs in the given table and their corresponding graph.

Step-5: Repeat steps 3&4 for next state of inputs and their corresponding outputs.

Step-6: Press the "Print" button after completing your simulation to get your results.

2) D flip flop

Step-1: Connect the supply(+5V) to the circuit.

Step-2: First press "ADD" button to add basic state of your output in the given table.

Step-3: Press the switches to select the required inputs "D" and "Clock".

Step-4: Press "ADD" button to add your inputs and outputs in the given table and their corresponding graph.

Step-5: Repeat step 3 & step 4 for next state of inputs and their corresponding outputs.

Step-6: Press the "Print" button after completing your simulation to get your results.

3) J-K flip flop

Step 1: Connect the supply (+5V) to the circuit.

Step-2: First press "ADD" button to add basic state of your output in the given table.

Step-3: Press the switches to select the required inputs "S" and "R" and apply the clock pulse.

Step-4: Press "ADD" button to add your inputs and outputs in the given table and their corresponding graph.

Step-5: Repeat step 3 & step 4 for next state of inputs and their corresponding outputs.

Step-6: Press the "Print" button after completing your simulation to get your results.

4) T flip flop

Step-1: Connect the supply(+5V) to the circuit.

Step-2: First press "ADD" button to add basic state of your output in the given table.

Step-3: Press the switches to select the required inputs "T" and apply the clock pulse.

Step-4: Press "ADD" button to add your inputs and outputs in the given table and their corresponding graph.

Step-5: Press the "Print" button after completing your simulation to get your results.

2.5. OBSERVATIONS:










Truth Table of RS Flip flop

S	R	Q	Action
0	0	No Change	Previous
0	1	0	Reset
1	0	1	Set
1	1	-	Forbidden

Truth Table of D Flip flop

Input			Output	
D	reset	clock	Q	Q'
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

Truth Table of JK flip flop

Trigger	Inputs		Output				Inference
			Present State		Next State		
CLK	J	K	Q	Q'	Q	Q'	
	x	x	-		-		Latched
	0	0	0	1	0	1	No Change
			1	0	1	0	
	0	1	0	1	0	1	Reset
			1	0	0	1	
	1	0	0	1	1	0	Set
			1	0	1	0	
	1	1	0	1	1	0	Toggles
			1	0	0	1	

Truth Table of T flip flop

T flip-flop

T	Clock	Q	Q'
0	↑	Q	Q'
1	↑	Q'	Q
x	↓	Q	Q'

2.6. RESULTS:

The truth table of different flip flops are verified.

2.7. VIVA VOCE:

- Which of the following is correct for a gated D-type flip-flop?
 - The Q output is either SET or RESET as soon as the D input goes HIGH or LOW
 - The output complement follows the input when enabled
 - Only one of the inputs can be HIGH at a time
 - The output toggles if one of the inputs is held HIGH
- A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?
 - AND or OR gates
 - Ex-OR or Ex-NOR gates
 - NOR or NAND gates
 - AND or NOR gate
- The truth table for an S-R flip-flop has how many valid entries?
 - 1
 - 2
 - 3
 - 4
- The flip-flops which has not any invalid states are _____

A) : S-R, J-K, D

B) S-R, J-K, T

B) J-K, D, S-R

D) J-K, D, T

5. Both the J-K & the T flip-flop are derived from the basic _____

A) S-R flip-flop

B) S-R latch

C) D latch

D) D flip-flop

EXPERIMENT - 3

POWER SUPPLY

Structure

3.1. OBJECT

3.2. APPARATUS USED

3.3. THEORY AND CIRCUIT DIAGRAM

3.4. GRAPH

3.5. OBSERVATION

3.6. RESULT

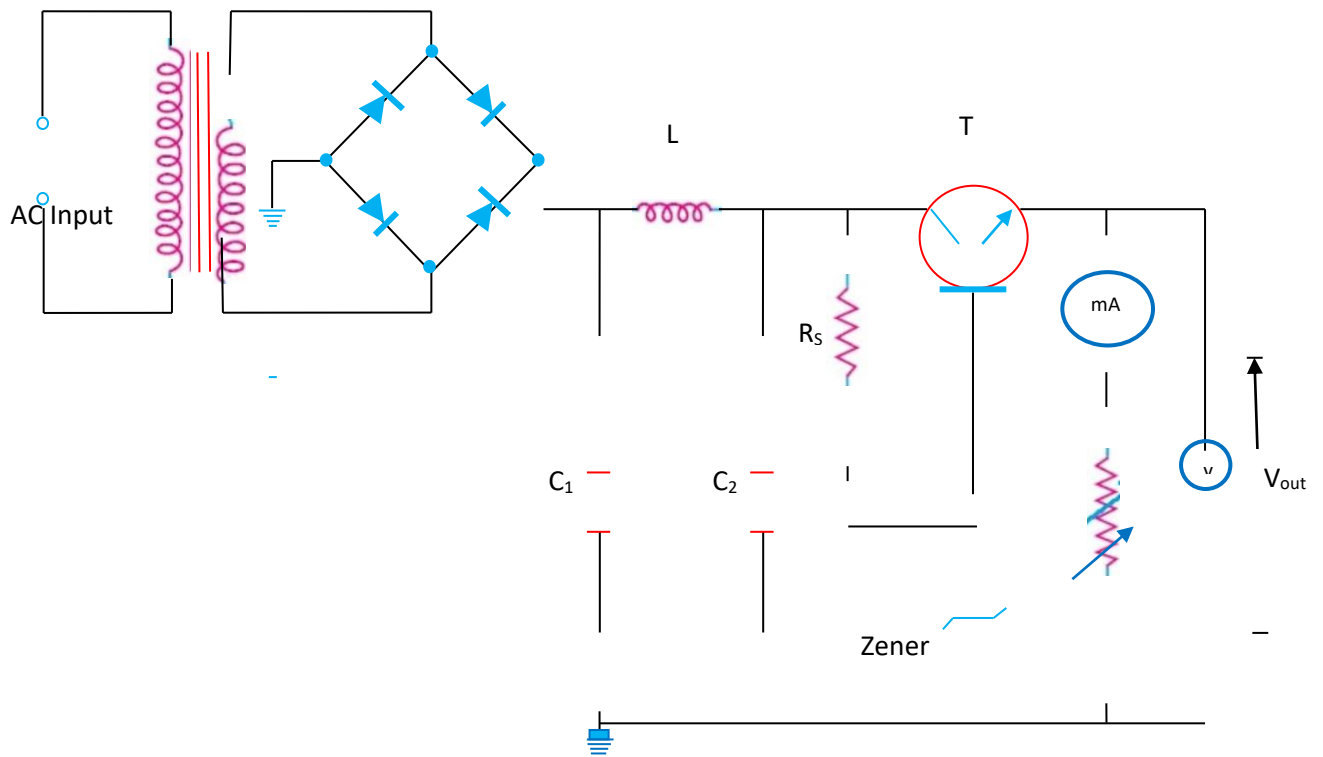
3.7. PRECAUTION

3.1. OBJECT: To study the characteristics of regulated DC Power supply.

3.2. APPARATUS USED: Variable AC source, Transformer, four diode, two capacitor, one inductor, one resistance, one transistor, dc voltmeter, milliammeter, variable resistor.

3.3. THEORY AND CIRCUIT DIAGRAM: A dc power supply is an electronic circuit which generates dc voltage using ac as input. If output of dc power supply remains unaltered under the variation of load current or input ac then it is called as regulated power supply. It has following components.

1. Step Down Transformer: It converts high ac voltage to low ac voltage.
2. Bridge Rectifier: It converts ac input voltage to dc voltage.
3. Filter Circuit: It reduces ripples which is present in output of rectifier.
4. Regulator Circuit: It regulates the output voltage of filter to be independent of variation in load current and input voltage.



3.4. GRAPH: Draw following graph

- 1) Input AC voltage verses output DC voltage
- 2) Output DC voltage verses load current at different input AC voltage

3.5. OBSERVATION:

1. Table for input AC voltage and output DC voltage.

Sr.No.	Input AC voltage (volt)	Output DC voltage (volt)
1	0	0
2	20	1.6
3	40	3.4
4	60	5.6
5	80	8.0
6	100	10.0
7	120	11.6
8	140	11.8
9	160	11.8
10	180	11.8
11	200	11.8
12	220	11.8

2. Table for output DC voltage with load current at different input AC voltage

Sr.No.	$V_{AC}=100$ volt		$V_{AC}=140$ volt		$V_{AC}=180$ volt		$V_{AC}=220$ volt	
	I_L (mA)	V_O (volt)	I_L (mA)	V_O (volt)	I_L (mA)	V_O (volt)	I_L (mA)	V_O (volt)
1	0	10.0	0	11.8	0	11.8	0	11.8
2	5	9.8	5	11.8	5	11.8	5	11.8
3	10	9.6	10	11.8	10	11.8	10	11.8
4	15	9.4	15	11.8	15	11.8	15	11.8
5	20	9.2	20	11.8	20	11.8	20	11.8
6	25	9.0	25	11.4	25	11.8	25	11.8
7	30	8.8	30	10.8	30	11.8	30	11.8
8	35	8.6	35	10.2	35	11.8	35	11.8
9	40	8.4	40	9.8	40	11.4	40	11.8
10	45	8.2	45	9.0	45	10.6	45	11.8
11	50	8.0	50	8.0	50	10.0	50	11.8

3.6. RESULT:

- 1.Graph 1 which you will draw using table 1 will show the output of given power supply is regulated for input AC voltage range 140-220 volts.
- 2.Graph 2 which you will draw using table 2 will show the output of given power supply is regulated for different range of load current at different AC input voltage.
- 3.Graph 2 will also indicate that the output of given power supply is regulated for full range of load current at 220 AC input voltage.

Thus, the output of a power supply is function input AC voltage and load current.

3.7. PRECAUTION:

- 1.Connections should be jointed correctly.
- 2.Connections must be tight.

Experiment 4

FIBER OPTICS

Structure

4.1 Aim

4.2 Objectives

4.3 Apparatus Used

4.4 Formula Used

4.5 Theory

4.6 Procedure

4.7 Observation

4.8 Result

4.9 Precaution And Source Of Error

4.10 Glossary

4.11 Viva-Voce Questions And Answers

4.12 References

EXPERIMENT NO.4 (A)

4.1 AIM To determine the numerical aperture of a given multimode optical fiber.

4.2 OBJECTIVE

- To illustrate the operation of optical fiber.
- To find the numerical aperture.

4.3 APPARATUS USED

Laser diode with power supply, microscope object (MO), V grooves with fiber holder, detector, multimode fiber, micro ammeter, post mount stand and screen etc.

4.4 FORMULA USED:

The numerical aperture (NA) is given by:

$$NA = \sin \Theta_0$$

Where Θ is the acceptance angle and can be written as:

$$\Theta_0 = \tan^{-1} (D/2d)$$

Here

D = Diameter of the spot produced on the screen.

d = Distance between the output end of the fiber and screen.

$NA = \sin \Theta_0 = \sin [\tan^{-1} (D/2d)]$
--

4.5 THEORY

Propagation of light

An optical fiber consists of a core that is surrounded by a cladding as schematically shown in figure 4.1.

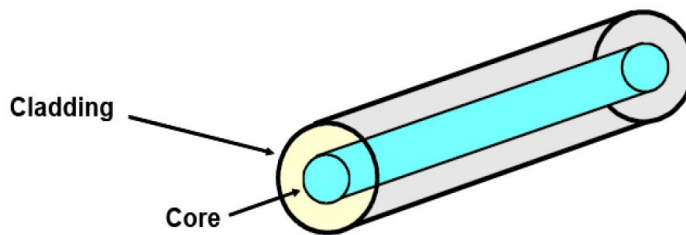


Figure 4.1: Core and cladding with refractive index n_1 and n_2 respectively.

The core is used for the transmission of optical signals and the cladding is for confining those signals within the core. The transmittance and reflection properties of a material depend on its refractive index. In order to guide the optical signals within the core of the fiber, the refractive index of the core (n_1) is deliberately kept higher than that of the cladding (n_2).

In order to understand the transmission process in more detail consider figure 4.2.

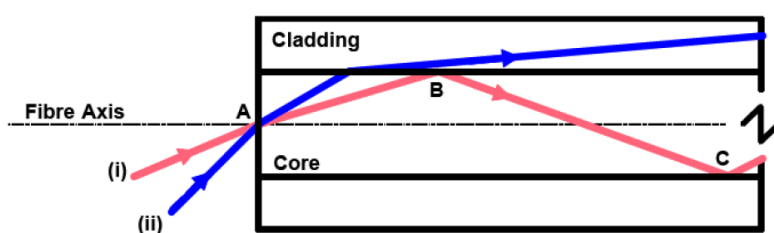
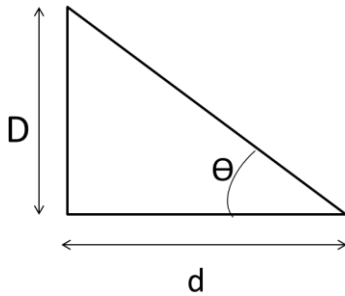


Figure 4.2: Propagation of light in an optical fiber.

The light ray (i) on entering the core at point A, reaches the core cladding boundary at point B, where it intersects the boundary at a small angle and reflects back in core at point C, resulting in **total internal reflection (TIR)** where the process of **TIR** is repeated.

If a ray enters the fiber at a steep angle (say light ray (ii)) then this ray intersects the core/cladding boundary at a larger angle than ray (i) which does not reflect back into the core and the losses in the cladding. This means that to be guided through a fiber a light ray must enter the core with an angle that is less than the angle called **Acceptance angle (Θ)** for the fiber.



Here

D = Diameter of the spot produced on the screen.

d = Distance between the output end of the fiber and screen.

It can be seen from above figure that acceptance angle of an optical fiber is given by the following relation:

$$\Theta = \tan^{-1}(D/2d)$$

A ray which enters the fiber with an angle greater than the acceptance angle will be lost in the cladding. By convention the acceptance angle for a fiber can also be described by the term "numerical aperture" as follows:

$$\text{Acceptance angle } (\Theta) = \sin^{-1}(\text{Numerical aperture (NA)})$$

Numerical aperture (NA)

It is a critical performance specification for multimode fibers. It indicates the maximum angle at which a particular fiber can accept the light that will be transmitted through it. Higher is the NA of the optical fiber, larger will be the cone of light that can be coupled into its core, as shown in figure 4.3:

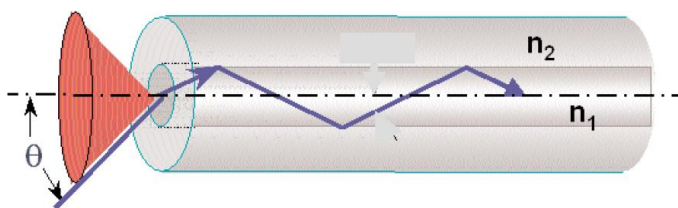


Figure 4.3: Numerical aperture defines the maximum angle (the “the cone of acceptance”) at which light can be launched into a fiber.

Multimode Fibers

Those fibers that carry more than one mode of light, because of its large acceptance angle (numerical aperture) are known as multimode fiber as shown in figure 4.4.

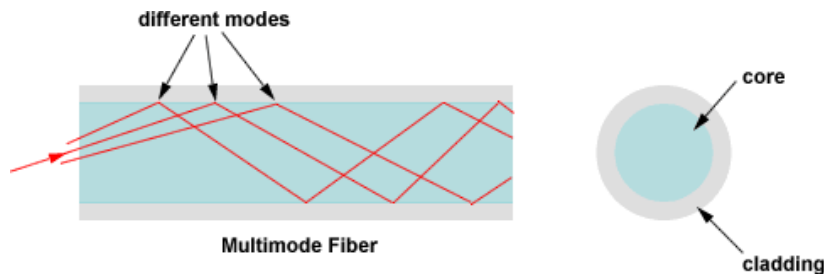


Figure 4.4: Illustration of multimode fiber carrying different modes of light ray.

From the above figure 4.4, it can be seen that there are several modes of light that enter the fiber with different angles to the fiber axis, up to the fiber's acceptance angle (numerical aperture) and larger the acceptance angle higher will be the no of modes that enters the fiber. Rays that enter with a shallower angle travel by a more direct path, and arrive sooner than those enter at steeper angles (which reflect many more times off the core/cladding boundaries as they travel the length of the fiber) and this arrival of different modes of the light at different times is called dispersion of modes or Modal dispersion.

Method: By Visual method

Experimental set up:

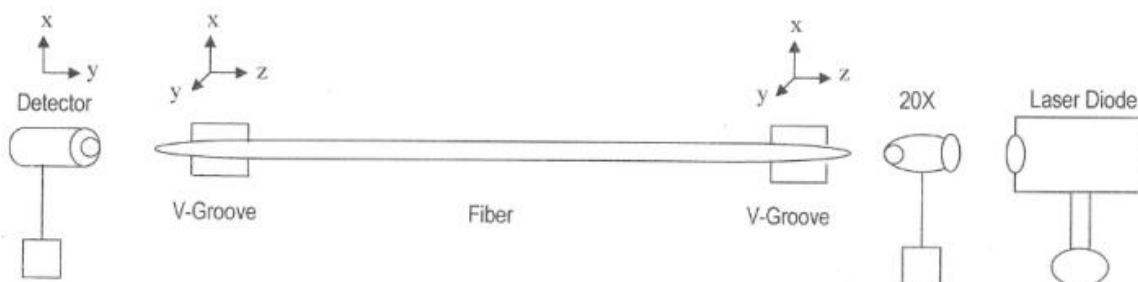


Figure 4.5: Experimental set up for the calculation of numerical aperture (NA)

4.6 PROCEDURE

This is a direct and quick estimation of numerical Aperture.

1. Draw the several concentric circles on a simple graph paper and paste it on one side of the screen by cello tape.
2. Replace the detector by screen placed normal to the fiber axis keeping the set-up same as in above figure. The screen is positioned in the far field in such as way that a line extending the axis of the fiber on the screen would have passed through the center of these circles drawn on the graph paper.
3. Adjust the fiber end which is mounted on the XYZ stake towards or away from the screen so that the emerging light spot fill completely one of the circles.
4. Note this diameter let us say it as say it as D1, which is measured accurately.
5. Repeat the experiment for other values of d (the distance between screen and the tip of the fiber) and calculate D2, D3, etc.
6. Calculate NA for different values of d i.e. Z+2 mm and then calculate the mean value of NA.

4.7 OBSERVATIONS

S. No.	Distance between the screen and the tip of the fiber (d) in mm	Diameter of the circle(D) in mm
1.		
2.		
3.		

Calculations:

$$NA = \sin \theta_0 = \sin [\tan^{-1} (D/2d)]$$

4.8 RESULTS

1. The Numerical Aperture of the given multimode fiber measured experimentally is -----.
2. The Numerical Aperture of the given multimode fiber measured given by manufacturer is

EXPERIMENT NO.4 (B)

4.1 OBJECTIVES To measure the power loss at a splice between two multimode fibers and to study the variation of splice loss with Longitudinal and Transverse misalignment of the given fibers.

4.2 OBJECTIVE

- To illustrate the operation of optical fiber.
- To find the numerical aperture.

4.3 APPARATUS USED

Trans and Long misalignment on post with all items as given in experiment no.4 (a).

4.4 FORMULA USED

Power loss/Coupling loss in decibels (dB) = $20 \log I_0 / I$

Where,

I_0 = Maximum current at the detectors end i.e. current at the minimum misalignment of given multimode fibers.

I = Current obtained at the detectors end for the subsequent misalignment.

4.5 THEORY

The power/ coupling loss is due to the attenuation of transmitting signal or light pulse. During transit light pulse lose some of their photons thus reducing their amplitude. Attenuation for a fiber is usually specified in decibels per kilometer. Power loss is by definition negative decibels. In common usage, discussions of power loss omit the negative sign. The basic measurement for power loss in a fiber is made by taking the logarithmic ratio of the input power (P_0) to the output power (P).

Power loss/Coupling loss in decibels (dB) = $10 \log_{10} P_0/P$

As power is directly proportional to the square of the current, hence power loss/Coupling loss can also be written as: Power loss/Coupling loss in decibels (dB) = $20 \log_{10} I_0/I$

4.6. PROCEDURE:

Experimental Set up:

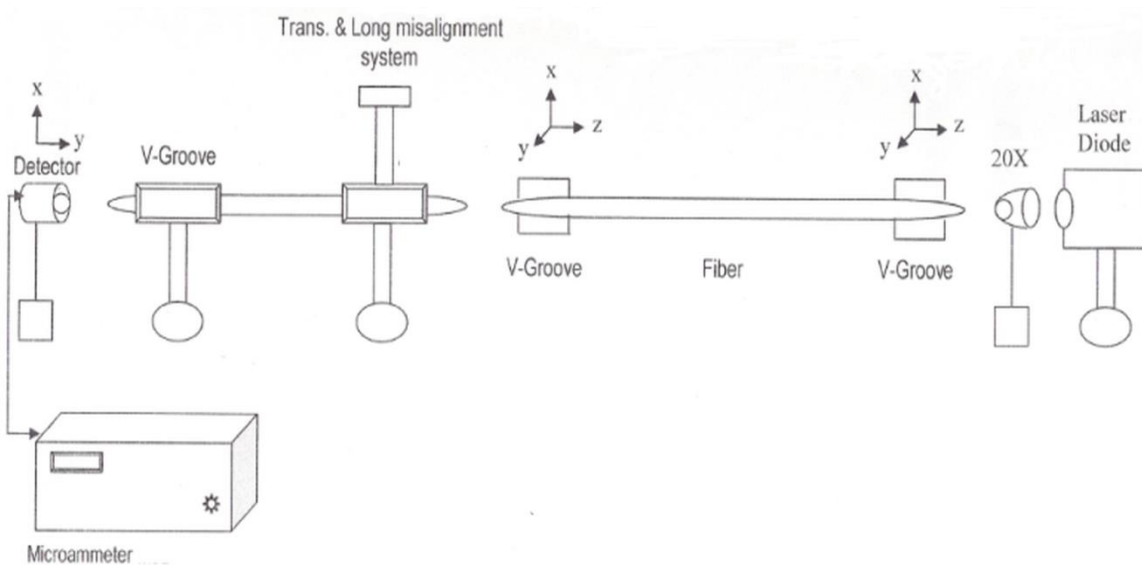


Figure 4.6: Experimental set up for the calculation of power loss at a splice between two multimode fibers.

Procedure:

1. Set the experiment schematically as shown in figure 8 as follows.
2. Take a second piece of multimode fiber, referred as receiving fiber.
3. Mount one end of the receiving fiber in the V groove on Trans and Long misalignment system and the other end of the fiber is coupled to a detector through the V groove mounted on the other post.
4. Align output end of the transmitting fiber mounted on X-Y-Z stack to the one end of the receiving fiber mounted on Trans and Long misalignment system with the help of X-Y-Z stack. And align other end of the receiving fiber to the detector with the help of X-Z stack to get maximum current in the micro ammeter. Note the current maximum current as I_0 .
5. **For Longitudinal misalignment**
Now the X-Y-Z stack on which the output end of the transmitting fiber is mounted

to induce longitudinal offset.

- (a) Move away the output end of the transmitting fiber by X-Y-Z stack into the field of view of the receiving fiber gradually to couple light from the transmitting fiber and micro ammeter through the detector.
- (b) The fiber could be moved in step of 1 mm of the graduated scale of X-Y-Z stack and measure the corresponding current in the micro ammeter for each setting of the fiber end. Record these readings in table as given below. Continue the measurement till the output current becomes zero.
- (c) Calculate the power loss as $\text{dB} = 20 \log I_0/I$
- (d) Plot a graph for longitudinal misalignment Vs power loss.

4.7. OBSERVATION

Observations for longitudinal misalignment:

Current at the minimum longitudinal misalignment $I_0 = \dots\dots\dots \mu\text{A}$

S. No.	Micrometer reading in mm (in Horizontal direction)	Corresponding detector current in (I) μA	Coupling loss in dB
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			

9.			
10.			
11.			
12.			
13.			
14.			
15.			
16.			
17.			
18.			
19.			
20.			
21.			
22.			
23.			

For Transverse Misalignment

Now the Trans and Long misalignment on which the input end of the receiving fiber is mounted is manipulated to induce Transverse offset. In actual practice for measuring transverse offset loss, it is recommended that the receiving fiber be moved away from the transmitting fiber (in transverse direction) till the micro ammeter reading reduced almost zero (i.e. register only ambient light).

(a) Again align the system to get the maximum current in micro ammeter I_0 .

- (b) Move the receiving input fiber's end gradually into the field of view of the transmitting fiber to couple light from the transmitting fiber to the micro ammeter through the detector.
- (c) The fiber could be moved in step of 0.25 mm of the graduated scale of micrometer fitted with the Trans and Long misalignment system and measure the corresponding current in the micro ammeter for each setting of the fiber end. Record these readings in table as given below. Continue the measurement till the output current becomes zero.
- (d) Calculate the power loss as $\text{dB} = 20 \log I_0 / I$
- (e) Plot a graph for Transverse misalignment Vs power loss.
- (f)

Observations for transverse misalignment:

Current at the minimum transverse misalignment $I_0 = \dots\dots\dots \mu\text{A}$

S. No.	Micrometer reading in mm (in Vertical direction)	Corresponding detector current in (I) μA	Coupling loss in dB
1.			
2.			
3.			
4.			
5.			

4.8. RESULTS:

- Graph shows the splice loss with Longitudinal and Transverse offset in a given fiber.
- These measurements would reveal that longitudinal offset is more tolerable off-set in terms of achieving a low loss fiber joint.

4.9 PRECAUTION AND SOURCE OF ERROR

1. The optical fiber cable should be free from twists and folds so as to avoid power loss.
2. Connections should be proper and tight.

4.10 GLOSSARY

Optical Fiber	a long thin thread of glass through which information, sound, data, etc. can be sent in the form of light
Multimode	able to operate in several modes
Power Loss	It is the difference between the input and output power of a device, apparatus, pump set, or process.
Acceptance angle	The acceptance angle of an optical fiber is the maximum incidence angle of a light ray which can be used for injecting light into a fiber core or waveguide.
Cladding	a covering or coating on a structure or material.
Single-mode fiber	It is a common type of optical fiber that is used to transmit over longer distances

4.11 VIVA-VOCE QUESTIONS AND ANSWERS

1. Distinguish between Critical and Acceptance angle.

Answer:

Critical angle: When a ray passes from a denser medium to rarer medium. It bends away from the normal. As the angle of incidence increases, refracted ray bends more and more away from the normal.

Acceptance angle: The maximum angle of incidence for which the ray propagates down the fiber is called as acceptance angle.

2. What do you understand by refractive index?

Answer: It measures the bending of a ray of light when passing from one medium into another.

3. What is the difference between reflection and refraction?

Answer:

Reflection	Refraction
Usually occurs in mirrors.	Usually occurs in Lenses.
Reflection can simply be defined as the reflection of light when it strikes the medium on a plane.	Refraction can be defined as the process of the shift of light when it passes through a medium leading to the bending of light.
The light entering the medium returns to the same direction.	The light entering the medium travels from one medium to another.
The angle of incidence of the light is equal to the angle of reflection.	The angle of incidence is not equal to the angle of reflection.

4. What is the basic principle of propagation of light in an optical fiber?

Answer: Optical fibers use total internal reflection to transmit light. It has a solid core of dense glass surrounded by a less dense cladding. The light ray passing through the inner core is reflected back instead of being refracted to the rarer cladding.

5. Define critical angle?

Answer: The critical angle is the angle of incidence, for which the angle of refraction is 90° .

6. What is Total Internal Reflection?

Answer: Total internal reflection is defined as the phenomenon which occurs when the light rays travel from a more optically denser medium to a less optically denser medium.

7. Name the two types of optical fiber?

Answer: There are two primary types of fiber – **multimode** and **singlemode**.

8. What are the advantages of optical fiber?

Answer: Advantages of Optical fiber:

- Greater bandwidth & faster speed.
- Cheap.
- Thinner and light-weighted
- Higher carrying capacity
- Less signal degradation
- Light signals
- Long lifespan

9. Give some applications of Graded-Index Multimode Optical Fiber.

Answer: The applications include the following:

- Generally, graded-index multimode fiber is used in comparatively less bandwidth and short-haul applications LANs (local area networks) which runs at 1 Gbps otherwise less.
- SMF or Step-index single-mode fiber is used in high BW and long haul applications like carrier backbones.

4.12 REFERENCES

1. Experiment (5) *Study of the properties of optical Fiber*, University of technology (Department Laser & Optoelectronics Engineering).
2. *Multimode Fiber (Multi Mode Fiber)* Fiber optics for sale .co, FOFS Wiki – Home (<http://www.fiberoptics4sale.com/Merchant2/multimode-fiber.php>)
3. *To measure propagation or attenuation loss in optical fiber* IIT delhi virtual labs Sakshat virtual lab (<http://iitd.vlab.co.in/?sub=65&brch=180&sim=309&cnt=1>)
4. Woodward, Bill and Emile B. Husson. *Fiber Optics and Technicians Installer Study Guide*. San Francisco: Sybex, 2005.
5. Downing, James. *Fiber Optic Communications*. Clifton Park: Thomson Delmar Learning, 2004.
6. Prakash, Satya. *Physics: Vol. 1,2*. City: V K Publications, 2008

EXPERIMENT 5: TO REALIZE AND STUDY OF SHIFT REGISTER

Structure

5.1 Aim

5.2 Objectives

5.3 Apparatus Used

5.4 Theory

5.5 Procedure

5.6 Result

5.7 Precaution and sources of error

5.8 Glossary

5.9 Viva-voce questions and Answers

5.10 References

5.1 AIM: To realize and study of Shift Register.

- 1) SISO (Serial in Serial out)
- 2) SIPO (Serial in Parallel out)
- 3) PIPO (Parallel in Parallel out)
- 4) PISO (Parallel in Serial out)

5.1 OBJECTIVES

- To illustrate the operation of shift registers
- To study different shift register configurations

5.3 APPARATUS USED

IC 7495, Patch Cords & IC Trainer Kit.

5.4 THEORY

A single bit of binary data may be stored in a flip flop (1 or 0). However, numerous flip flops are required to hold multiple bits of data. To hold n bits of data, N flip flops must be linked in a specific order. A register is a device that is used to store this type of data. It consists of a sequence of flip flops used to hold numerous bits of data.

With the use of shift registers, the information held in these registers may be transferred. Shift registers are a form of sequential logic circuit used mostly for data storage. They are a series of flip-flops linked together in a chain, with the output of one flip-flop becoming the input of the next. A single clock controls all of the flip-flops, and they are all set or reset at the same time.

“Shift left registers” are the registers that shift the bits to the left.

“Shift right registers” are the registers that shift the bits to the right.

Shift registers are basically of 4 types. These are:

- **Serial-in to Parallel-out (SIPO)** - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
- **Serial-in to Serial-out (SISO)** - the data is shifted serially in and out of the register, one bit at a time in either a left or right direction under clock control.
- **Parallel-in to Serial-out (PISO)** - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- **Parallel-in to Parallel-out (PIPO)** - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

Serial-In Serial-Out Shift Register (SISO):

Serial-In Serial-Out shift register is a shift register that accepts serial input (one bit at a time over a single data line) and outputs serial data. The data exits the shift register one bit at a time in a serial pattern since there is only one output, thus the term Serial-In Serial-Out Shift Register.

A serial-in serial-out shift register is shown in the logic circuit below. The circuit is made up of four D flip-flops linked in a serial fashion. Because each flip flop receives the same clock signal, they are all synchronised with one another.

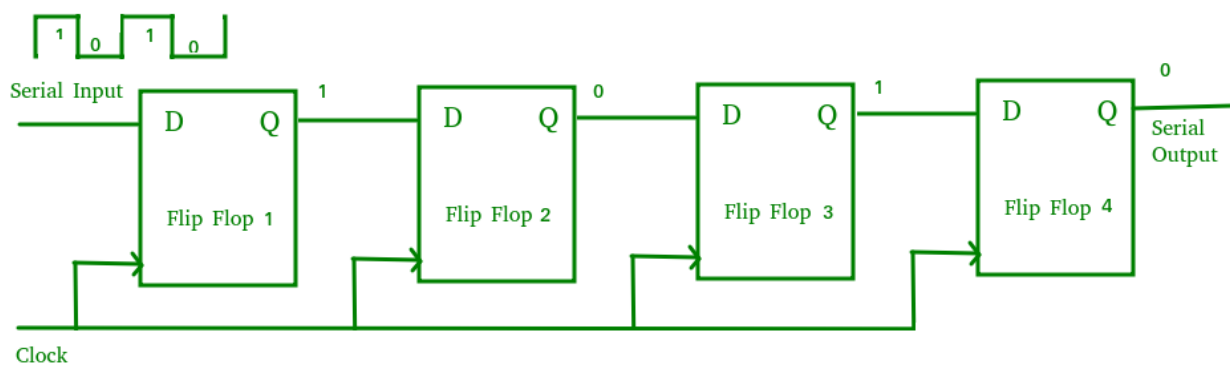


Figure 5.1: Serial-In Serial-Out Shift Register.

The above circuit is an example of a shift right register, which accepts serial data from the flip flop's left side. A SISO's principal function is to act as a delay element.

Output Waveform

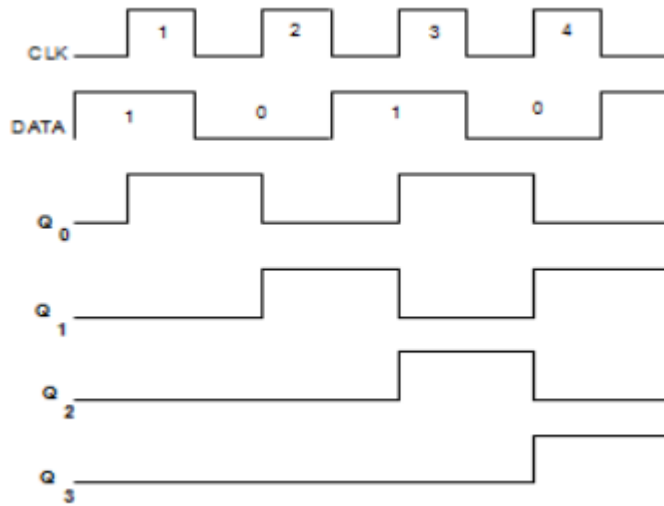


Figure 5.2: Output waveforms of 4-bit Serial In Serial Out register.

Truth Table:

CLK	Serial In	Serial OUT
1	1	0
2	0	0
3	0	0
4	1	1
5	X	0
6	X	0
7	X	1

Serial-In Parallel-Out shift Register (SIPO)

A Serial-In Parallel-Out shift register accepts serial input (one bit at a time over a single data line) and creates a parallel output.

A serial-in-parallel-out shift register is shown in the logic circuit below. The circuit is made up of four D flip-flops that are linked together. To RESET the flip flops, the clear (CLR) signal is supplied to them in addition to the clock signal. The first flip flop's output is connected to the second flip flop's input, and so on. Because each flip flop receives the same clock signal, they are all synchronised with one another.

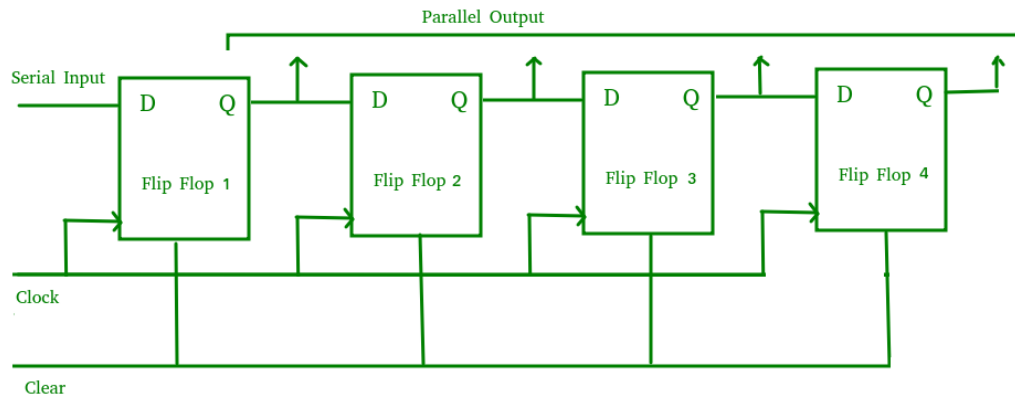


Figure 5.3: Serial-In parallel-Out Shift Register

The circuit of a shift right register is shown above. It takes serial data from the flip flop's left side and produces a parallel output. Because the principal application of the SIPO register is to transform serial data into parallel data, they are utilised in communication lines when demultiplexing of a data line into numerous parallel lines is necessary.

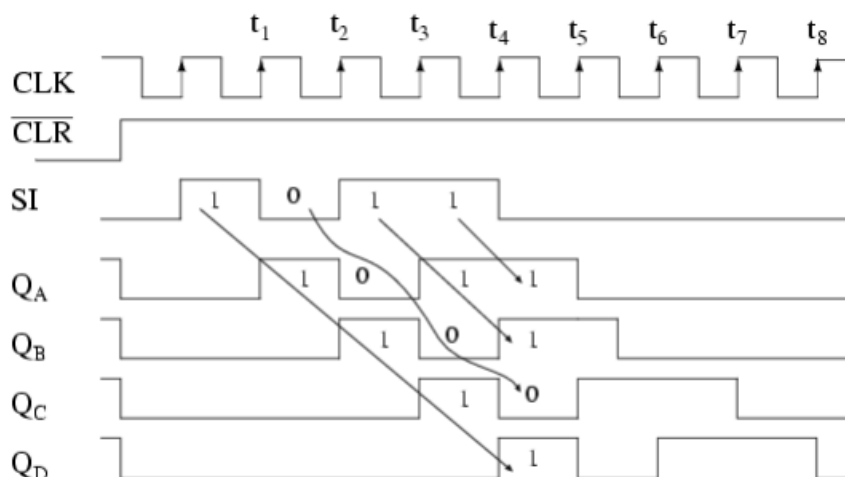


Figure 5.4: Output waveforms of 4-bit Serial In Parallel Out register.

Truth Table:

CLK	DATA	OUTPUT			
		Q _A	Q _B	Q _C	Q _D
1	1	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	1
4	1	1	0	0	1

Parallel-In Serial-Out Shift Register (PISO) –

Parallel-In Serial-Out shift registers allow parallel input (data is delivered independently to each flip flop and in a simultaneous way) and create a serial output.

A parallel-in-serial-out shift register is shown in the logic circuit below. The circuit is made up of four D flip-flops that are linked together. The clock input is linked to all of the flip flops directly, while the input data is connected to each flip flop separately through a multiplexer at the input of each flip flop. The preceding flip flop's output and parallel data input are linked to the MUX's input, while the MUX's output is connected to the next flip flop. All of these flip-flops are in harmony

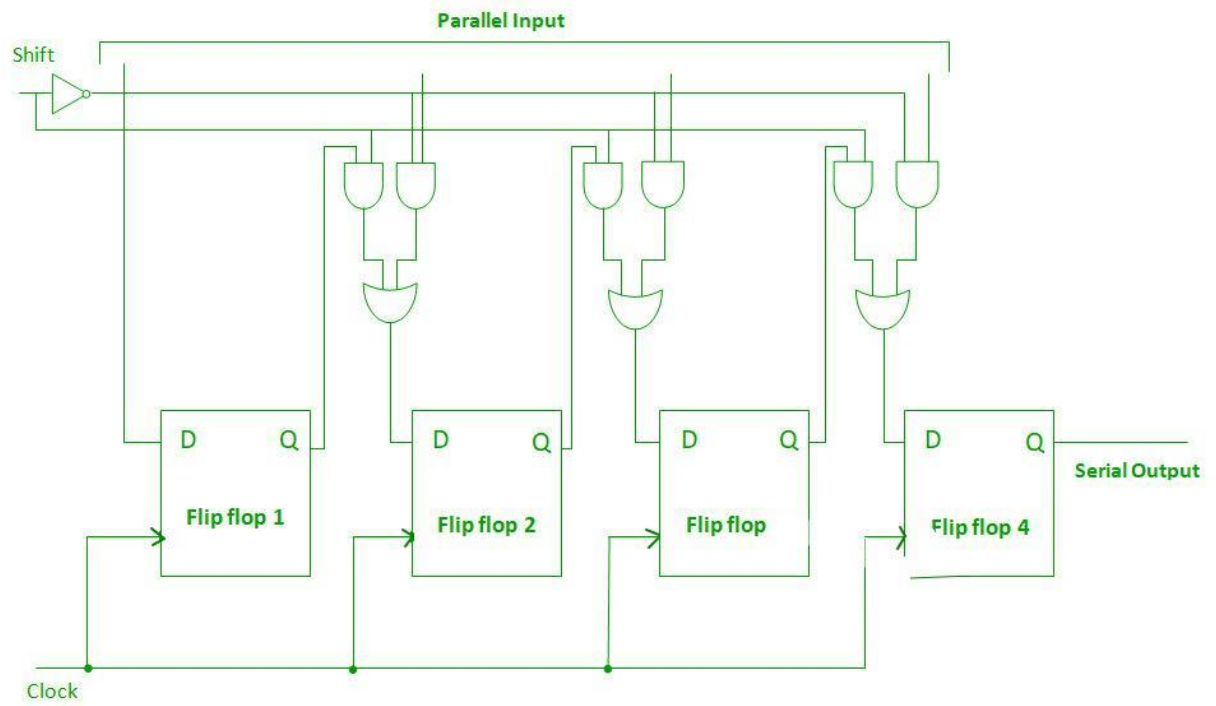


Figure 5.5: Parallel -In Serial-Out Shift Register.

To convert parallel data to serial data, a Parallel in Serial Out (PISO) shift register is utilised.

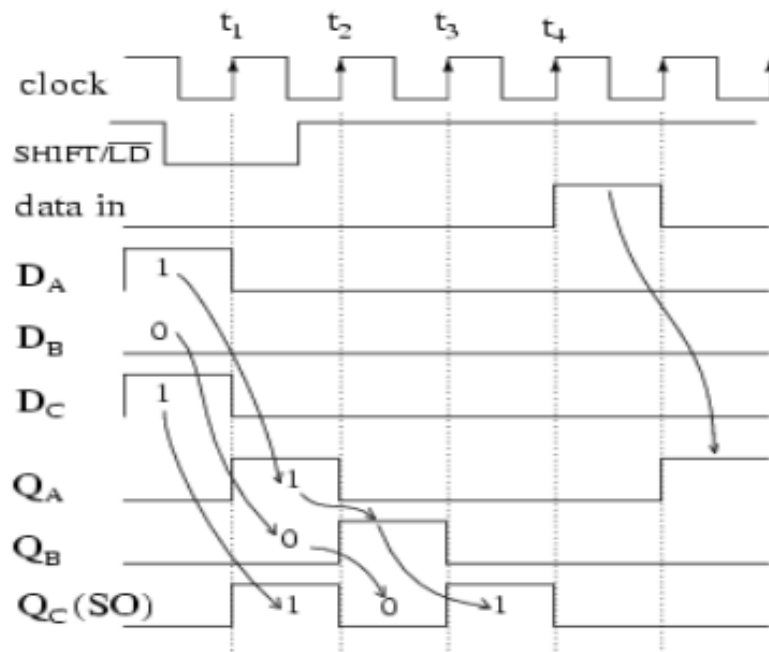


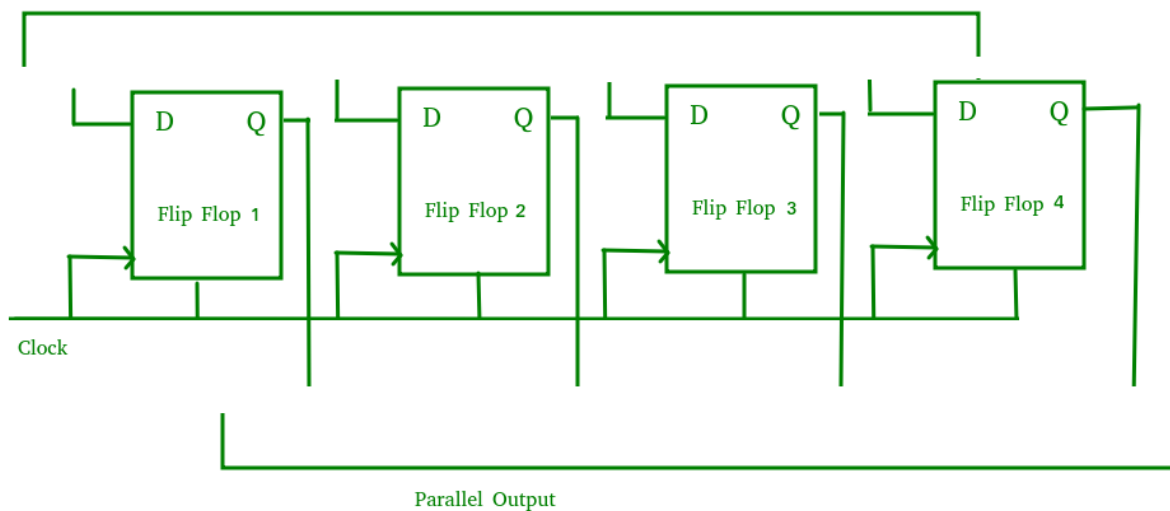
Figure 5.6: Output Waveform of Parallel-In Serial-Out Shift Register.**Truth Table:**

CLK	Q ₃	Q ₂	Q ₁	Q ₀	O/P
0	1	0	0	1	1
1	0	0	0	0	0
2	0	0	0	0	0
3	0	0	0	0	1

PIPO (Parallel-In Parallel-Out Shift Register) —

Parallel-In parallel-Out shift register is a shift register that permits parallel input (data is delivered independently to each flip flop and in a simultaneous way) and also provides a parallel output.

A parallel-in-parallel-out shift register is shown in the logic circuit below. The circuit is made up of four D flip-flops that are linked together. All four flip flops are linked to the clear (CLR) and clock signals. Because no serial shifting of data is necessary, there are no linkages between the individual flip-flops in this sort of register. Data is delivered to each flip flop independently as input, and output is similarly gathered separately from each flip flop.

**Figure 5.7: Parallel -In Parallel-Out Shift Register.**

A PIPO shift register, like a SISO shift register, is utilised as a temporary storage device and also works as a delay element.

Truth Table:

CLK	DATA INPUT				OUTPUT			
	D _A	D _B	D _C	D _D	Q _A	Q _B	Q _C	Q _D
1	1	0	0	1	1	0	0	1
2	1	0	1	0	1	0	1	0

APPLICATIONS OF SHIFT REGISTERS:

- Shift registers are utilised for data transport and manipulation as well as temporary data storage.
- Digital circuits are time delayed using serial-in serial-out and parallel-in parallel-out shift registers.
- Shift registers are used to store temporary data.
- Data transport and manipulation are also done with shift registers.
- The serial-in parallel-out shift register is used in communication lines where demultiplexing of a data stream into many parallel lines is required.
- To convert parallel data to serial data, a Parallel in Serial out shift register is employed.

5.5 PROCEDURE

Pin diagram of IC 7495 is shown in the below mentioned Figure 15.8.

PIN DIAGRAM of IC 7495:

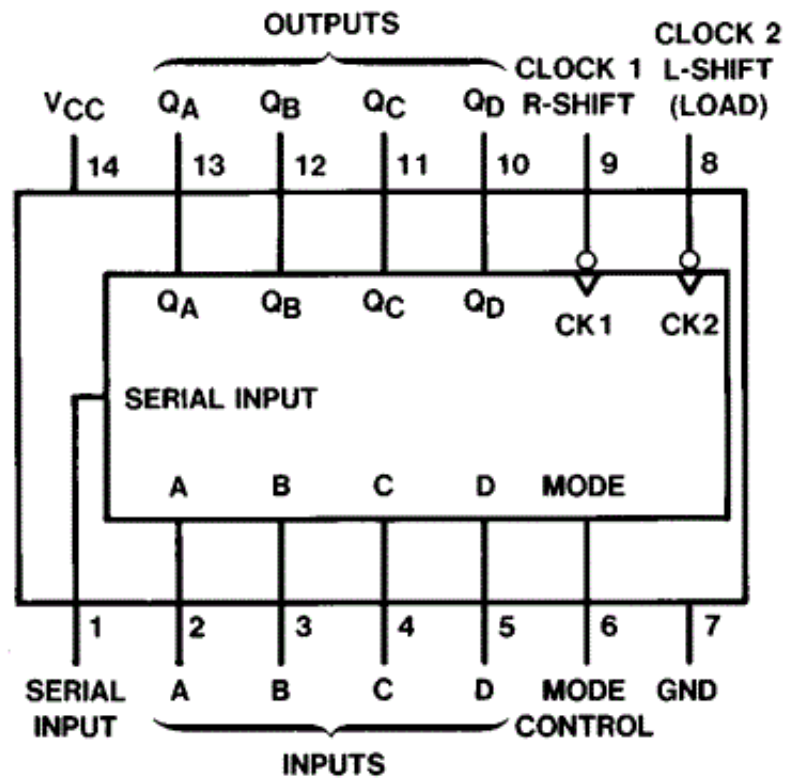


Figure 5.8: PIN DIAGRAM of IC 7495.

Serial In Serial Out (SISO):

1. Connections are made as per circuit diagram.
2. Load the shift register with 4 bits of data one by one serially.
3. At the end of 4th clock pulse the first data 'd0' appears at QD.
4. Apply another clock pulse; the second data 'd1' appears at QD.
5. Apply another clock pulse; the third data appears at QD.
6. Application of next clock pulse will enable the 4th data 'd3' to appear at QD. Thus the data applied serially at the input comes out serially at QD.

Logic Diagram

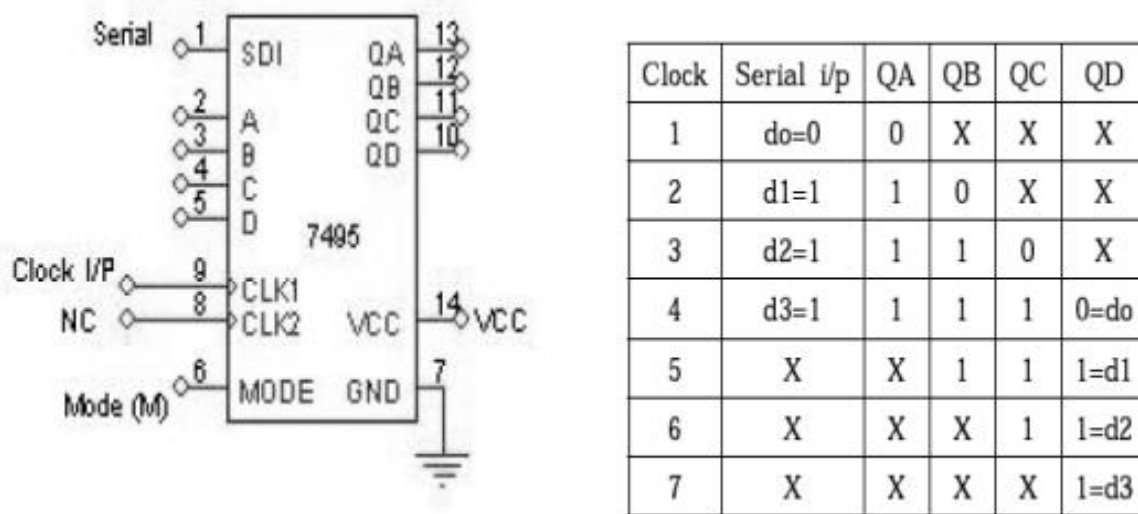


Figure 5.9:Serial In Serial Out (SISO)

Serial In Parallel Out (SIPO):

1. Connections are made as per circuit diagram.
2. Apply the data at serial i/p
3. Apply one clock pulse at clock 1 (Right Shift) observe this data at QA.
4. Apply the next data at serial i/p.
5. Apply one clock pulse at clock 2, observe that the data on QA will shift to QB and the new data applied will appear at QA.
6. Repeat steps 2 and 3 till all the 4 bits data are entered one by one into the shift register.

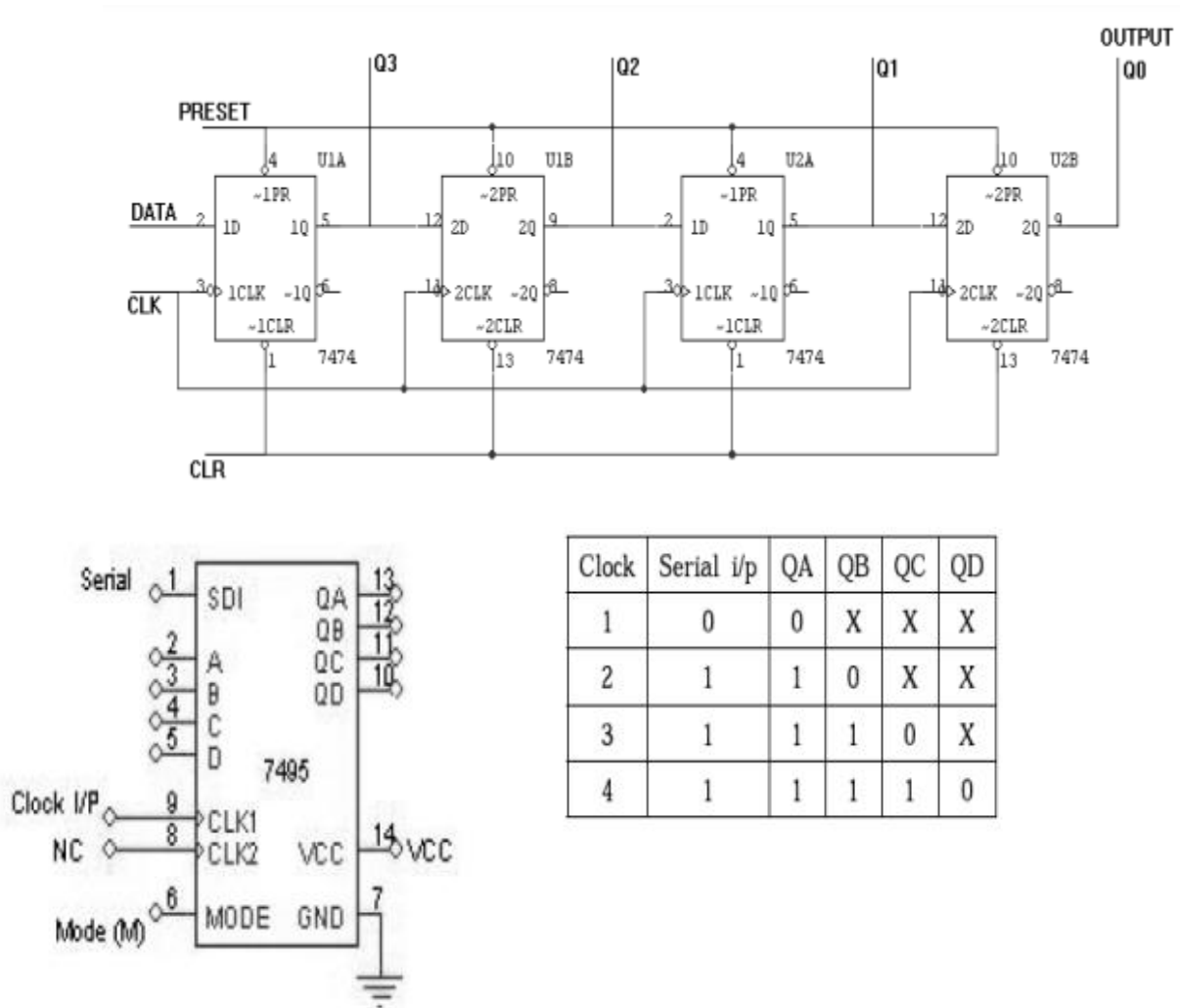
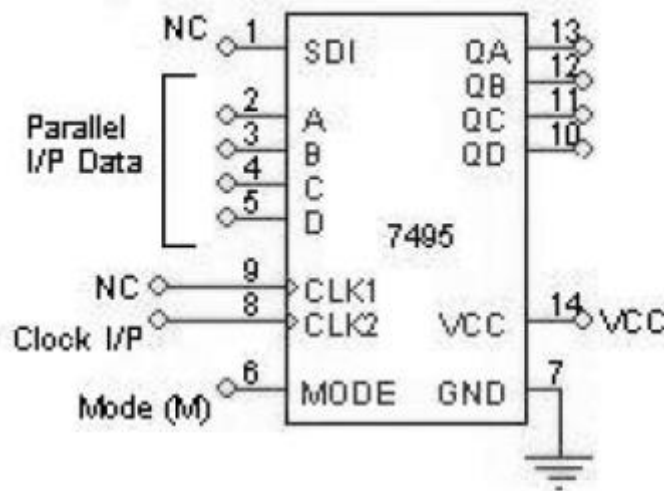
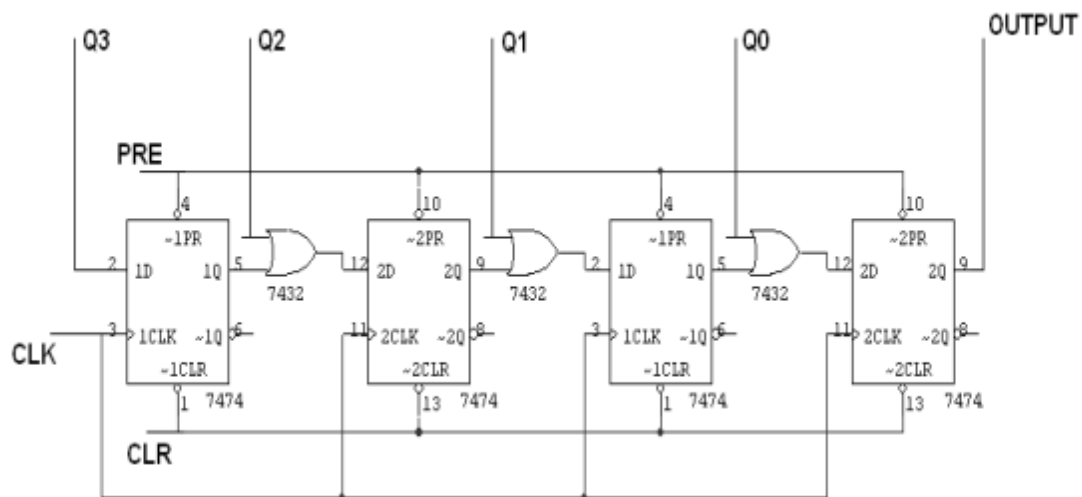


Figure 5.10:Serial In Parallel Out (SIPO)

Parallel In Serial Out (PISO):

1. Connections are made as per circuit diagram.
2. Apply the desired 4 bit data at A, B, C and D.
3. Keeping the mode control M=1 apply one clock pulse. The data applied at A, B, C and D will appear at QA, QB, QC and QD respectively.
4. Now mode control M=0. Apply clock pulses one by one and observe the Data coming out serially at QD



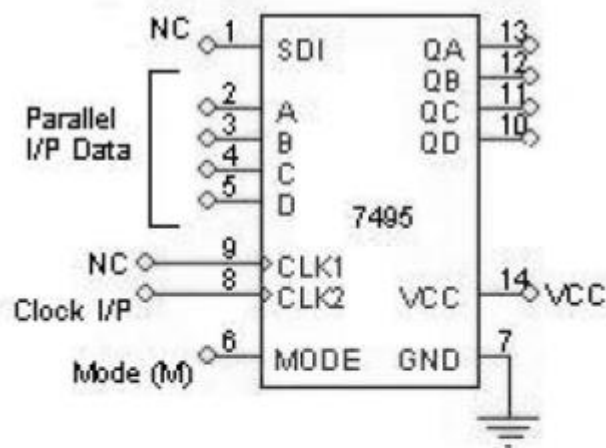
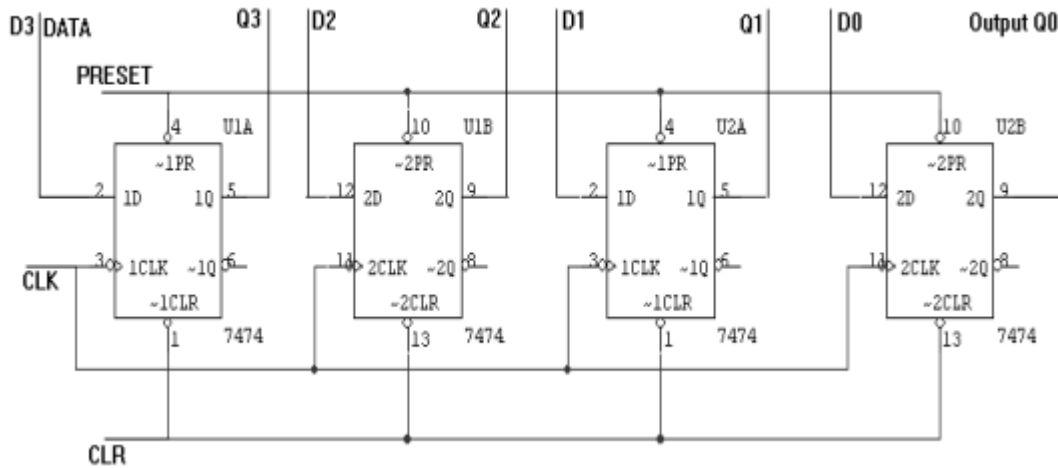
Mode	Clock	Parallel i/p				Parallel o/p			
		A	B	C	D	QA	QB	QC	QD
1	1	1	0	1	1	1	0	1	1
0	2	X	X	X	X	X	1	0	1
0	3	X	X	X	X	X	X	1	0
0	4	X	X	X	X	X	X	X	1

Figure 5.11: Parallel In Serial Out (PISO)

Parallel In Parallel Out (PIPO):

1. Connections are made as per circuit diagram.

2. Apply the 4 bit data at A, B, C and D.
3. Apply one clock pulse at Clock 2 (Note: Mode control M=1).
4. The 4 bit data at A, B, C and D appears at QA, QB, QC and QD respectively.



Clock	Parallel i/p				Parallel o/p			
	A	B	C	D	QA	QB	QC	QD
1	1	0	1	1	1	0	1	1

Figure 5.12: Parallel In Parallel Out (PIPO)

5.6 RESULT

Shift registers using IC 7495 in all its modes i.e. SIPO/SISO, PISO/PIPO are verified.

5.7 PRECAUTIONS AND SOURCES OF ERROR

1. All the connections should be made properly.
2. Connect the ground first then connect the Vcc.
3. Main voltage should be kept switched off, while making connections.
4. Digital kit should be handled with utmost care.
5. Circuit should be off before change the connections.
6. We should switch off the power supply after completing experiment.
7. We should not touch the naked wire.

5.8 GLOSSARY

Bit	The smallest increment of data on a computer
Binary	The digits 0 and 1 - to store data
Register	Type of computer memory used to quickly accept, store, and transfer data and instructions that are being used immediately by the CPU
Data	Information that has been translated into a form that is efficient for movement or processing
IC	An assembly of electronic components, fabricated as a single unit, in which miniaturized active devices
Flip flop	A device which stores a single bit (binary digit) of data
Sequential circuit	A logic circuit whose outputs at a specified time are a function of the inputs at that time, and also at a finite number of preceding times.

5.9 VIVA-VOCE QUESTIONS AND ANSWERS

1. What is a register?

Answer:Registers are a sort of computer memory that is used to accept, store, and transport data and instructions that are needed by the CPU right away.

2. What are the applications of register?

Answer:Application of Register:

- Registers are used to store data in digital form, but they may also hold data and addresses.
- Registers are also employed in the manufacture of digital memory chips such as ROM chips and Flash memory.
- Registers are also used to create cache memory in the CPU.

3. Explain the term Single bit register.

Answer:A Register is a collection of flip flops. A flip flop is used to store single bit digital data. For storing a large number of bits, the storage capacity is increased by grouping more than one flip flops.

4. How data is transferred in the shift register?

Answer:A shift register is a sort of digital circuit employing a cascade of flip-flops and the output of one flip-flop is linked to the input of the next. They are connected by a single clock signal, which causes the data in the system to move from one place to another.

5. Describe the function of shift register.

Answer:The function of the shift register is to store binary words.

6. Describe the methods of data transfer from the input to the output in the shift register.

Answer:Data Transfer in the shift register

- Serial in serial out
- Parallel in parallel out
- Serial in parallel out
- Parallel in serial out

7. Which type of flip flop is used in the shift register in order to avoid timing problems?

Answer: To avoid timing issues in the shift register, an edge triggered or master slave flip flop is utilised.

8. Describe the difference between shift register and counter.

Answer:Shift register: It is used for storage and transfer of digital data and has no specific sequence of states.

Counter: It has specific sequence of states.

5.10 REFERENCES

1. M. Morris Mano, “Digital Logic and Computer Design”,Pearson
2. https://www.electronicstutorials.ws/sequential/seq_5.html

(L)

EXPERIMENT 6 STUDY OF ENCODER AND DECODER

Structure

6.1 Aim

6.2 Objectives

6.3 Apparatus Used

6.4 Theory

6.5 Procedure

6.6 Result

6.7 Precaution and sources of error

6.8 Glossary

6.9 Viva-voce questions and Answers

6.10 References

(L)

6.1 AIM

To analyse the truth table of 4 X 2 decoder using NOT (7404) and AND (7408) logic gate ICs and 2 X 4 encoder using OR (7432) logic gate IC and to understand the working of 4 X 2 decoder and 2 X 4 encoder circuit with the help of LEDs display.

6.2 OBJECTIVES

1. Understanding the construction and operational principles of digital decoders and encoders.
2. To be familiar with basics of conversion from binary to decimal by using decoder networks.
3. To learn about various applications of decoder and encoder.

6.3 APPRATUS USED

IC-7447, 74147, LED, Digital IC trainer kit and Patch chords.

6.4THEORY

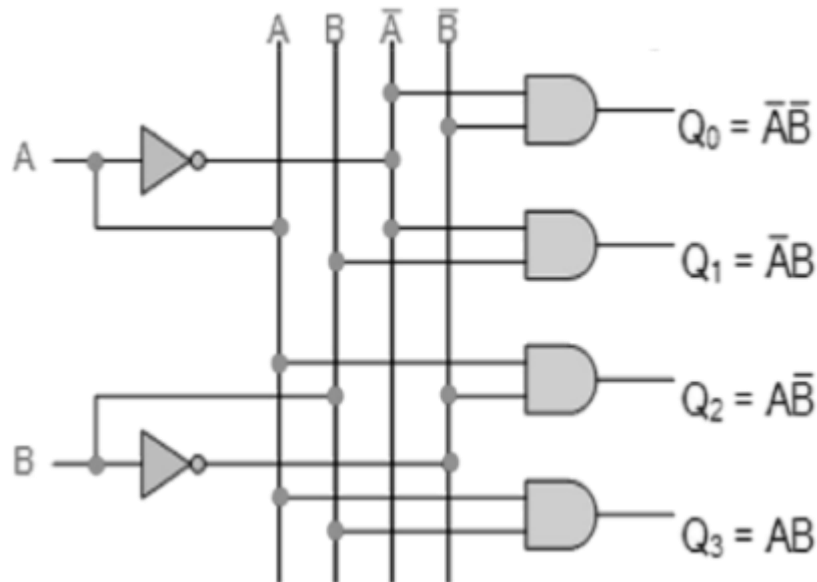
Decoders and encoders are crucial components in digital electrical projects. It is used to transform data from one format to another. These are often used in communication systems such as telephony, networking, and data transmission from one end to the other. It is also employed in the digital world for simple data transfer, where it is combined with codes and then sent. The coded data is gathered from the code at the receiver's end and then processed for display. Now we will see what is aDecoder is, how it works, and how it may be used.

Decoders:

A decoder is a logic circuit that that detects whether a binary number or word is present. The input to the decoder is a parallel binary number and the output is abinary signal that indicates the presence or absence of that specific number.It is a combinational circuit that converts binary information from n input lines to amaximum of 2^n unique output line.

Decoders have a wide variety of applications in digital systems such as data demultiplexing, digital display, digital to analog converting, memory addressing, etc.

(L)

2-to-4 line Decoder**Figure 6.1: Circuit Diagram of 2-to-4 Decoder.**

An array of four AND gates makes up the 2-to-4 line binary decoder, which is shown in the Figure. The 2-to-4 binary decoder decodes two binary inputs labeled A and B into one of four outputs, hence the name. Each output corresponds to one of the two input variables' minterms (each output Equals a minterm).

The binary inputs A and B select which of the output lines from Q0 to Q3 is "HIGH" at logic level "1," while the remaining outputs are "LOW" at logic level "0," allowing just one output to be active (HIGH) at any given moment.

(L)

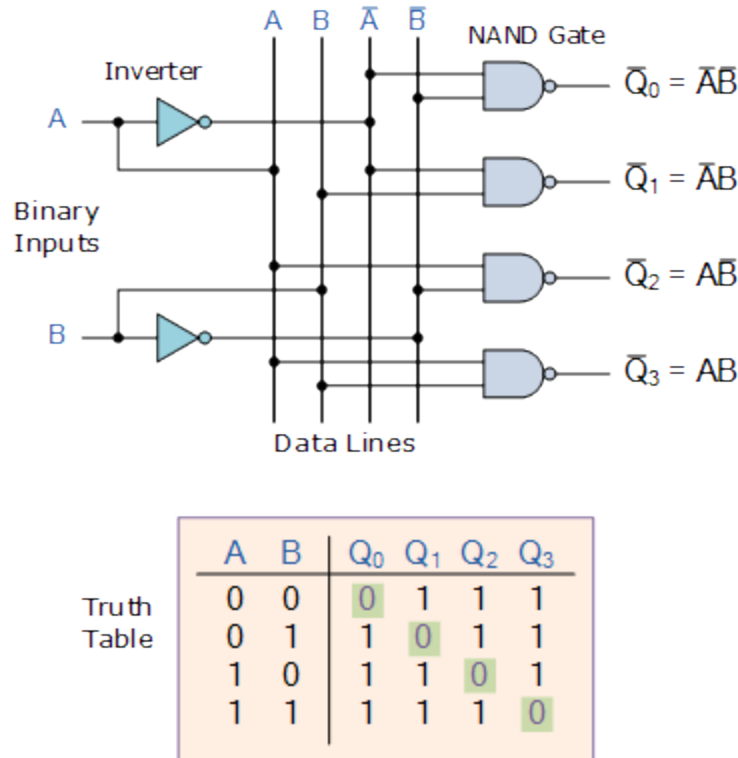


Figure 6.2. Logic Diagram and Truth table of 2-to-4 Decoder.

As a result, whatever output line is marked "HIGH" identifies the binary code present at the input, or "decodes" the binary input. An additional input pin labelled "Enable" on some binary decoders controls the device's outputs.

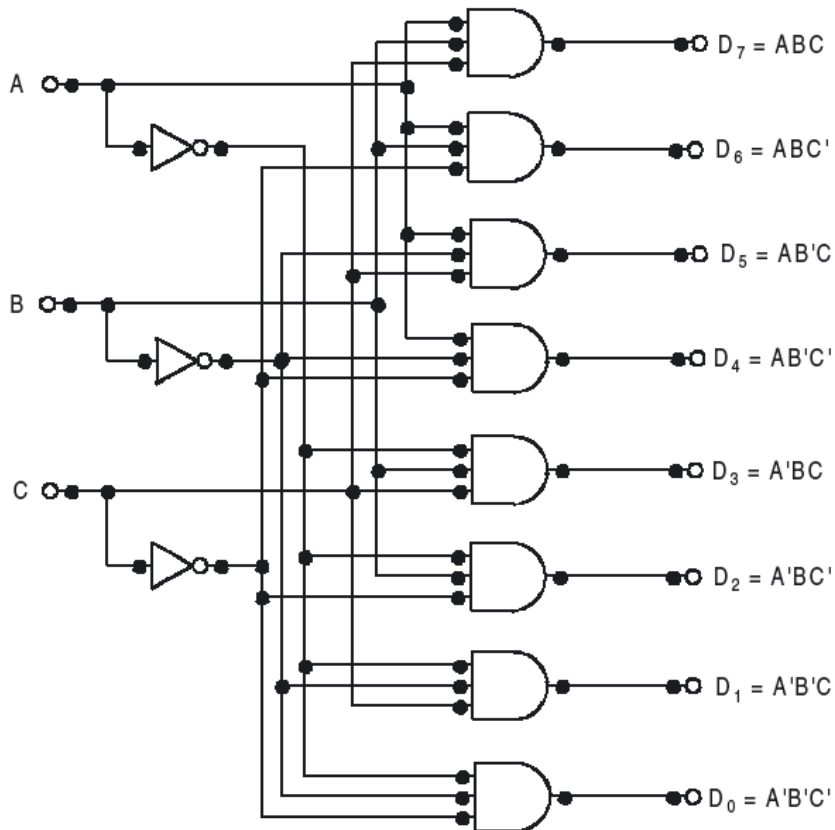
This additional input allows the outputs of the decoder to be turned "ON" or "OFF" as needed. When the Enable input is set to 1, output is created; otherwise, all outputs are 0. The implementation only needs to be tweaked slightly: the Enable input is passed into the AND gates that generate the outputs.

When Enable is set to 0, all AND gates receive a 0 as one of their inputs, resulting in no output. When Enable is 1, one of the AND gates' inputs is set to 1, and the output is determined by the remaining inputs. As a result, the decoder's output is determined by whether Enable is set to high or low.

3-to-8 line decoder

A 3-to-8 line decoder is illustrated in Figure 6.3.

(L)



Input variables			Outputs							
A	B	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Figure 6.3: A 3-to-8 line decoder.

(L)

The 3-to-8 line decoder consists of three input variables and eight output lines. Note that each of the output lines represents one of the minterms generated from three variables. The internal combinational circuit is realized with the help of INVERTER gates and AND gates. The operation of the decoder circuit may be further illustrated from the input output relationship as given in the above table. Note that the output variables are mutually exclusive to each other, as only one output is possible to be logic 1 at any one time.

BCD-to-Seven Segment decoder:

A seven segment LED display contains 7 LEDs. Each LED is called a segment and they are identified as (a, b, c, d, e, f, g) segments.

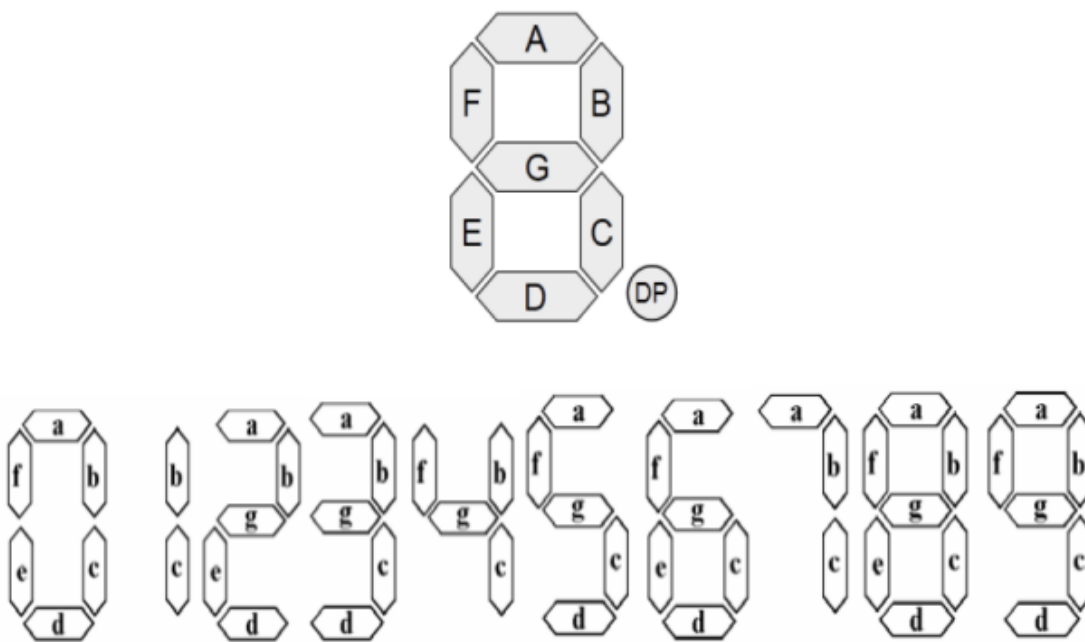


Figure 6.4: A seven segment LED display.

For example, if decimal 9 is to be displayed, a, b, c, d, f, g must be 0 and the others must be 1, while decimal 5 requires a, f, g, c, d to be 0 and the others to be 1.

(L)

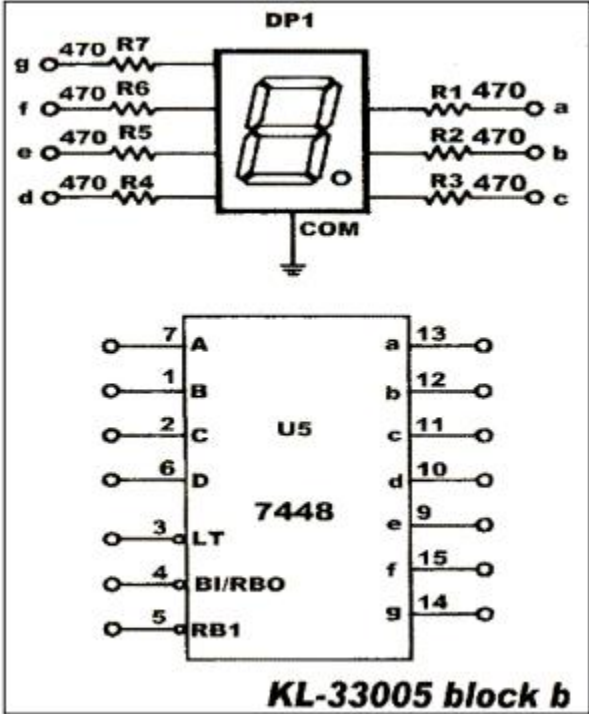
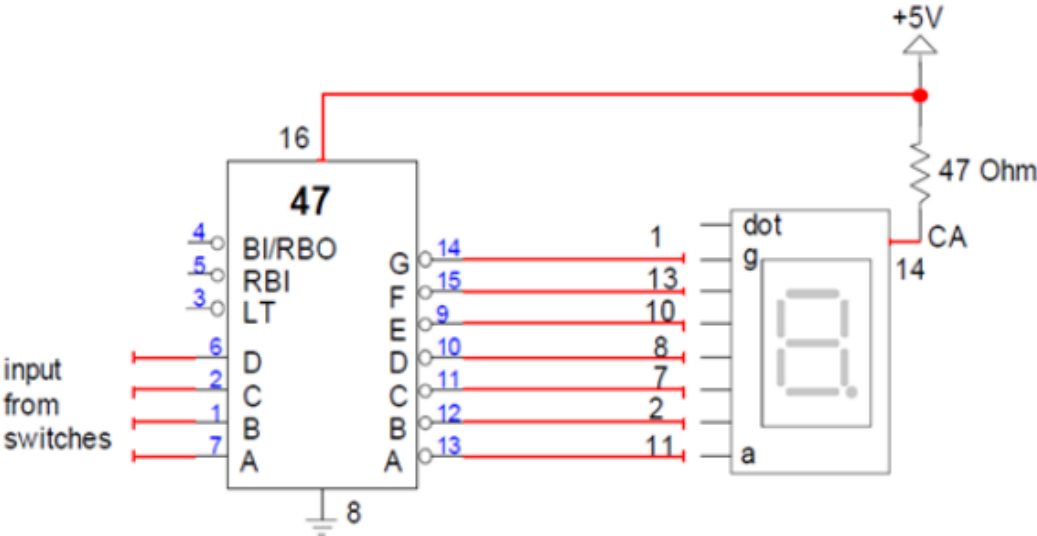


Figure 6.5: BCD to seven segment Decoder and 7-segment display.

Application of Decoders:

1. Decoders are used to input data to a specified output line as is done in addressing core memory where input data is to be stored in a specified memory location.

(L)

2. Used in code conversion
3. Used for data distribution in Demultiplexing.
4. They are used in high performance memory coding or data routing application requiring very short propagation delay times.
5. Decoders can be used as timing or sequencing signals to turn devices on or off at specific times, because when the decoder inputs come from a counter that is being continually pulsed, the decoder outputs will be activated sequentially.

Encoders:

The reverse process of the decoder is performed by an encoder, which is a combinational network. An encoder has n input lines and 2^n or fewer output lines. The binary code for the 2^n input variables is generated by the encoder's output lines.

4-to-2 line Encoder

The 4 to 2 Encoder consists of four inputs Y_3, Y_2, Y_1 & Y_0 and two outputs A_1 & A_0 . At any time, only one of these 4 inputs can be '1' in order to get the respective binary code at the output.

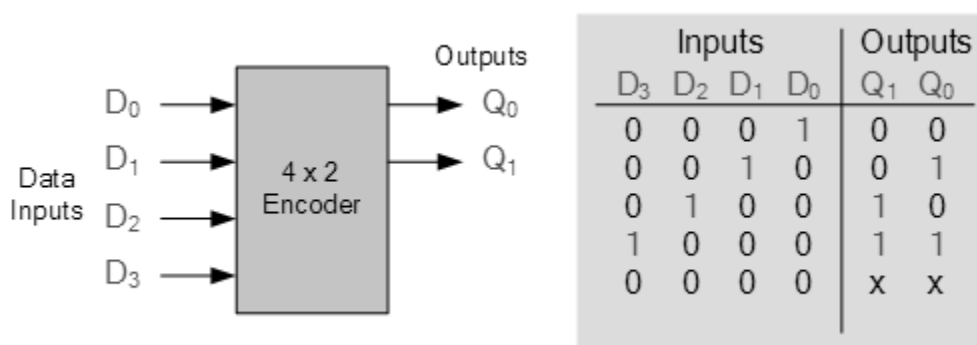


Figure 6.6: Logic symbol and truth table of 4 to 2 encoder.

(L)

8-to-3 line Encoder

Figure 6.7 shows an encoder with eight inputs and three outputs. It's also known as an octal-to-binary encoder, because it generates binary codes at outputs based on the input conditions. The truth table can be found below.

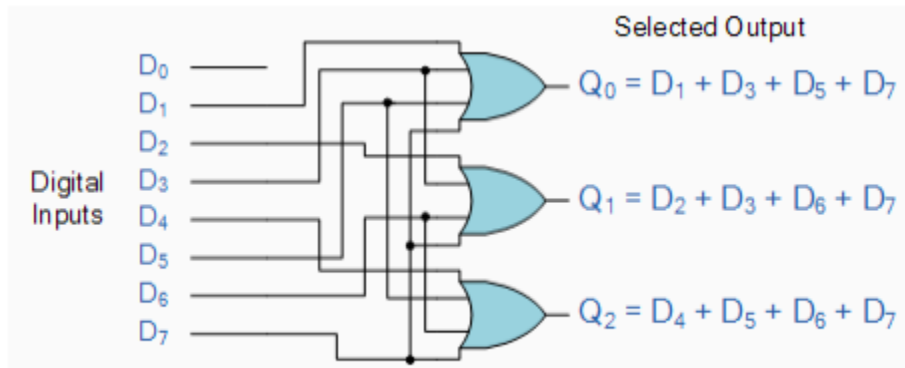


Figure 6.7: Circuit Diagram of 8-to-3 line Encoder.

Encoder requires that only one input line is activated to logic 1 at any given moment; otherwise, the other circuit is meaningless. It's worth noting that there are $2^8 = 256$ potential possibilities for eight inputs, but only eight are useful, and the rest are don't-care situations. It's also worth noting that the D_0 input isn't linked to any of the gates. In this situation, all of the binary outputs Q_2 , Q_1 , and Q_0 must be 0s. If all of the input variables D_0 to D_7 are logic 0, the output will be all 0s. This is the circuit's most significant flaw. This difference can be resolved by providing a new output that indicates that all of the previous outputs have been removed.

However, because it is difficult to build with OR gates and only a small number of gates are needed, this sort of encoder is not available in an IC package. A priority encoder is the sort of encoder found in the IC package. These encoders use an input priority system to ensure that only the most important data is encoded. If both D_2 and D_4 inputs are logic 1 at the same time, the output will be based only on D_4 , i.e., output will be 100.

(L)

Inputs								Outputs		
D0	D1	D2	D3	D4	D5	D6	D7	Q2	Q1	Q0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

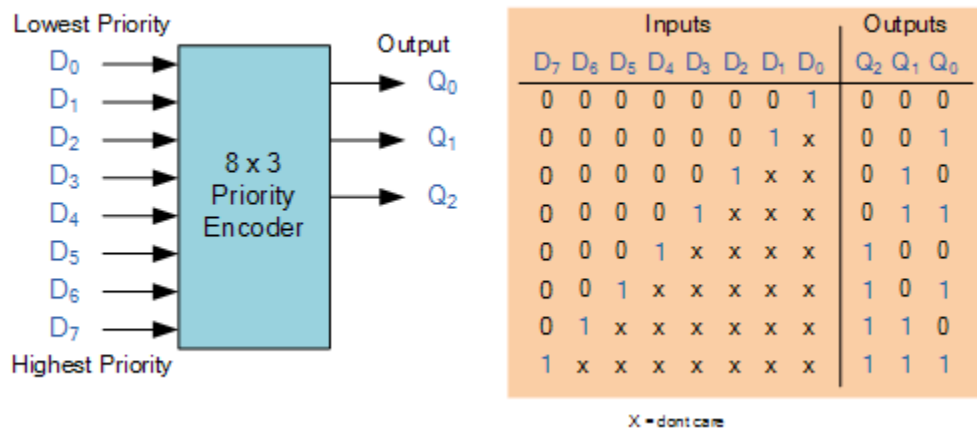


Figure 6.8:A8-to-3 line Encoder.

Applications of Encoder:

Applications of Encoder is listed below.

1. Automatic health monitoring systems.
2. RF-based home automation system.
3. Robotics vehicle with the metal detector.
4. War field flying robot with a using night-vision flying camera.
5. Speed synchronization of multiple motors in industries.
6. Encoder for CNC machines.
7. Encoder for the medical industry most common for breast cancer treatment in the world.

(L)

8. Encoder for the electronics industry.

6.5 PROCEDURE

Part I

To make a 2-to-4 decoder, connect inputs A and B to data switches SW0 and SW1, and outputs F1, F2, F3, and F4 to LEDs L0, L1, L2, and L3, respectively.

Then test the outcomes.

Part II

Use KL-33005 block b to construct BCD-to-Seven Segment, connect inputs A, B, C and D to data switches, connect the input (LT) to DIP1.0 and set it to logic 1, connect outputs of BCD to Seven Segment and from Seven Segment to the Leds. Then complete this table.

INPUTS				7- Segments							Display number
A	B	C	D	a	b	c	d	e	f	g	
0	0	0	0								
0	0	0	1								
0	0	1	0								
0	0	1	1								
0	1	0	0								
0	1	0	1								
0	1	1	0								
0	1	1	1								
1	0	0	0								
1	0	0	1								

6.6 RESULT

The truth table of 4 X 2 decoder and 2 X 4 encoder have been verified.

6.7 PRECAUTION AND SOURCES OF ERROR

(L)

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The Vcc and ground should be applied carefully at the specified pin only.

6.8 GLOSSARY

Decoder	A device that changes electronic signals into a form that can be understood
Encoder	It is a device or process that converts data from one format to another.
Data	Facts or information
Logic circuit	A circuit for performing logical operations on input signals.
Signal	To notify by a motion, action, movement, or sound
LED	A device that produces a light on electrical and electronic equipment
Digital	Using an electronic system that uses the numbers 1 and 0 to record sound or store information, and that gives high-quality results

6.9 VIVA-VOCE QUESTIONS AND ANSWERS

1. What is a priority encoder?

Answer: A priority encoder is a circuit or method that reduces the number of outputs from numerous binary inputs. The binary representation of the index of the most significant active line, beginning from zero, is the output of a priority encoder.

2. What are the advantages of an encoder?

Answer: There are a number of advantages of an Encoder. Some of them are mentioned below:

- Highly reliable and accurate
- Low-cost feedback
- High resolution
- Integrated electronics
- Fuses optical and digital technology
- Can be incorporated into existing applications

(L)

3. What is the disadvantages of an encoder?

Answer: There are a number of disadvantages of an Encoder. Some of them are mentioned below:

- Subject to magnetic or radio interference (Magnetic Encoders)
- Direct light source interference (Optical Encoders)
- Susceptible to dirt, oil and dust contaminates

4. What are some application of decoders?

Answer:The following are some applications of decoder:

- It is utilised in the conversion of codes. i.e. the analog to digital conversion in the analog decoder.
- It can also be used to distribute data.
- This decode can be used to reduce the impact of system decoding in a high-performance memory system.
- The decoders are utilised in CPU memory location identification as address decoders.
- It can also be used to transform instructions into CPU control signals in electrical circuits.
- They are mostly employed in data transport and logical circuits.
- They may also be used to make simple digital logics such as half adders and full adders, as well as other digital designs.
- Different I/O devices are selected by the microprocessor.
- It converts binary data into text.

5. What is the difference between encoder and decoder?

Answer:Both an encoder and a decoder are combinational logic circuits; however, an encoder produces binary code as its output, whilst a decoder does not. A decoder, on the other hand, takes binary code as input.

A device that turns an active data signal into a coded message format is known as an encoder. A decoder, on the other hand, reverses the encoder's function and turns the coded data into the original data.

(L)

Multiple choice based questions:

1. A decoder converts n inputs to ____ outputs

a: n^n

b: n

c: n^2

d: 2^n

2. BCD to 7 segment conversion in a _____

a: Comparing process

b: None of the answers

c: Encoding process

d: Decoding process

3. Decoders and Encoders are doing reverse operation.

a: True

b: False

c: may be

d: may not be

4. Which of the following are building block of the Encoders?

a: OR Gate

b: AND Gate

c: NOT Gate

d: NAND Gate

5. A circuit that changes a code into a set of signals is called

a: encoder

b: decoder

c: multiplexer

d: data selector

(L)

ANSWER: 1: d), 2:d), 3: a), 4: a), 5: b)

6.10 REFERENCES

1. M. Morris Mano, Michael D Ciletti, "Digital Design", Pearson, 4th ed. 2008
2. William Gothmann H, Digital Electronics : An Introduction To Theory And Practice , Prentice Hall, 2nd ed. 1982
3. S Salivahanan, S Arivazhagan, "Digital Circuits and Design", Vikas Publishing House Pvt Ltd., 3rd ed. 2009
4. Ronald J. Tocci, Neal S. Widmer, Gregory L. Moss, "Digital Systems", Pearson, 10th ed. 2009
5. Thomas L. Floyd, R. P. Jain, "Digital Fundamentals", Pearson, 11th ed. 2017
6. Encoder and Decoder: <https://www.youtube.com/watch?v=-KEh2xVsYQ4>
7. 4:2 Encoder Circuit Working: <https://www.youtube.com/watch?v=sKMH9dgqPdU>
8. Encoders and Decoders: <https://www.geeksforgeeks.org/digital-logic-encoders-decoders/>
9. Anil K. Maini, "Digital Electronics: Principles, Devices and Applications", Wiley-Blackwell, 2007

(L)

EXPERIMENT -7 MULTIPLEXER AND DEMULTIPLEXER

7.1. OBJECT: To demonstrate a basic Multiplexer / Demultiplexer system, and become familiar with different types of multiplexers and demultiplexer.

7.2. THEORY

7.2.1. MULTIPLEXER: It is not necessary to use only discrete gates (AND, OR, NAND, NOR, EXOR, EXNOR) in the design of the combinational logic circuit, with the availability of the medium scale integrated (MSI) and large scale integrated (LSI), it is possible to design a very complicated circuits with a simple procedure, for example it is waste of time in most cases to try to minimize combinational logic circuit which has eight input using tabular method, while it will simpler if we used multiplexers.

A multiplexer is a network that has many inputs and one output, and the value of the output will be the value of one of inputs which will be decided by some select lines. The simplest type of multiplexer is the two lines to one line data multiplexer. Let A be one of the inputs and B is the other input and Y is the output as in Fig. (1), and S is the select line, then

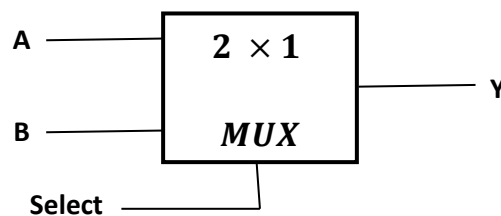
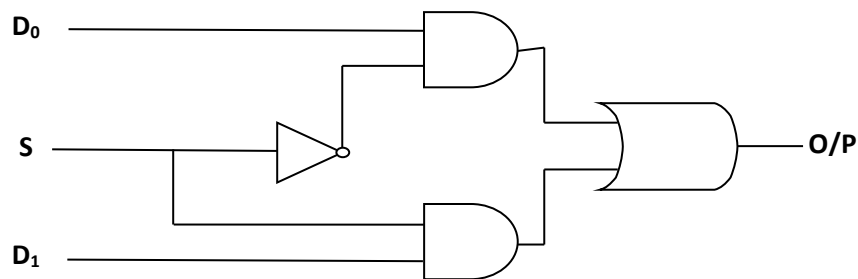


FIG: 7.1.

(L)

Two to One Line Multiplexer $Y = A$ if Select = 0. $Y = B$ if Select = 1.

The logic circuit diagram of the Two to One line Multiplexer is shown in Fig. 6.2.

**FIG: 7.2.****7.2.1.1. LOGIC CIRCUIT OF TWO TO ONE LINE MULTIPLEXER:**

There are many 2 to 1 data selector as an MSI, for example (7498, 74157, 74158) which contains four (quadruple) two-to-one data selectors in one chip. To use the multiplexer in the design of combinational logic circuit, usually the truth table or K-map of function is used in which the table or the map is divided into 2, 4, 8, or 16 equal parts according to the type of multiplexer used. Some of the inputs of the combinational circuit is connected directly to the select lines while data lines of the multiplexer will be a function to the other inputs according to the sum map or sub tables.

There are other types of multiplexers 4to1 line, 8to1 line, and 16to1 line multiplexer, and the number of select lines of these multiplexer are 2, 3, and 4 lines respectively. Fig.6.3. shows the four to one line multiplexer and its function block diagram.

Example:

(L)

Design the following expression using multiplexer.

$$F(A, B, C) = AC + BC + ABC\bar{C}$$

Solution:

Number of variables = 3, it is better to use 4to1 line multiplexer, i.e.:

Number of selection lines = Number of variable -1.

The truth table of the function is shown below:

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

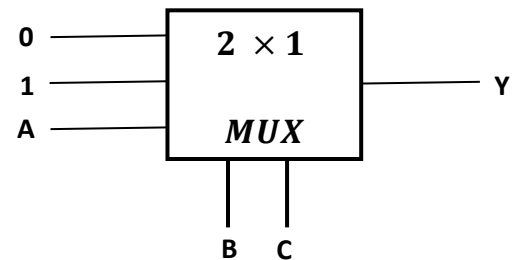
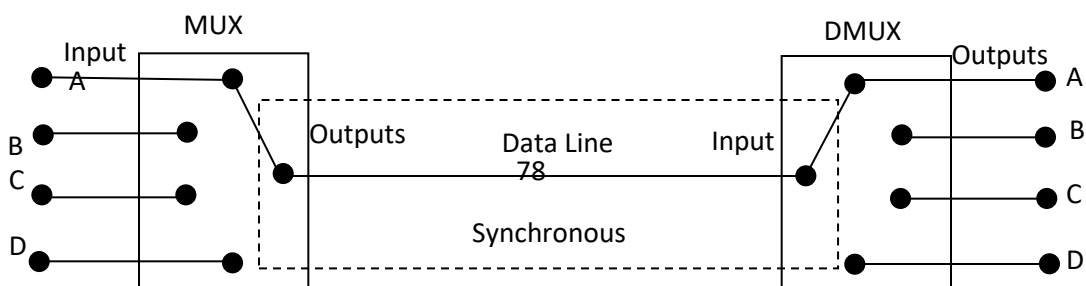


TABLE: 7.1

7.2.2. DEMULTIPLEXER: A demultiplexer basically reverse the multiplexing function. It is taken data from one line and distribute them to given number of output lines. Fig. (3) shown a one-to-four-line demultiplexer circuit. The input data line goes to all of the AND gates. The two select lines enable only one gate at a time and the data appearing on the input line will pass through the selected gate to the associated output line.

The simplest type of demultiplexer is the one to two lines DMUX. as shown in Fig. 6.4.



(L)

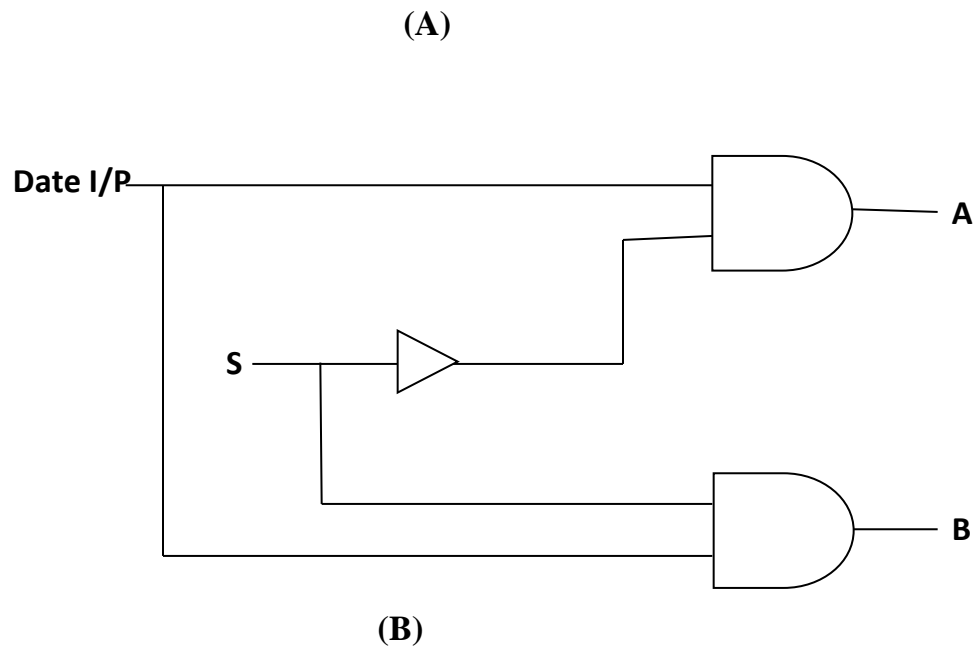


FIG. 7.4. MUX/DMUX System (A) Switch Analog (B) LOGIC GATE CIRCUIT

7.3. PROCEDURE:

1. Connect the circuit as shown in FIG. 7.2.
2. Apply a signal to (A) input from clock (High Speed) of the logic INTIKIT unit. Draw the wave form.
3. Apply signal to (B) input from the pulse generator of amplitude = 5 Volt (p-p) frequency = 50 KHz. Draw the wave form.
4. Set the selector control input ($S = 0$), draw the output waveform from the multiplexer.
5. Set $S = 1$, draw the output waveform of the multiplexer.

(L)

6. Connect the output of MUX to the DMUX circuit of Fig. (5) and find the output of demultiplexer when $S = 0$ and when $S = 1$.

7.4. DISCUSSION:

1. Construct 8×1 MUX by using 2×1 MUX.
2. Construct 16×1 MUX by using 4×1 MUX and 2×4 Decoder.
3. Give some applications for the Multiplexer.
4. How many chips of 2×1 MUX you will need if you want to design 16×1 MUX.
5. Design the following expression using multiplexer: $F(A,B,C) = \overline{A} \overline{B} + AC$

Put the selection circuit $S_1, S_0 = AC, AB, BC$.

(L)

EXPERIMENT 8: TO REALIZE ONE & TWO BIT COMPARATOR AND STUDY OF 7485 MAGNITUDE COMPARATOR

Structure

8.1 AIM

8.2 OBJECTIVES

8.3 APPARATUS USED

8.4 THEORY

8.5 PROCEDURE

8.6 RESULT

8.7 PRECAUTION AND SOURCE OF ERROR

8.8 GLOSSARY

8.9 VIVA-VOCE QUESTIONS AND ANSWERS

8.10 REFERENCES

(L)

8.1 AIM

To realize One & Two Bit Comparator and study of 7485 magnitude comparator.

8.2 OBJECTIVE

- To illustrate the operation of magnitude comparator
- To study different comparator configurations

8.3 APPARATUS USED

AND gate, X-OR gate, OR gate, NOT gate, IC 7485

8.4 THEORY

Digital or binary comparators are made up of typical AND, NOR, and NOT gates that compare digital signals at their input terminals and provide an output based on the state of those inputs.

For example, we need to be able to compare binary numbers and decide whether the value of input A is higher than, lower than, or equal to the value of input B, among other things. The digital comparator achieves this by employing a series of logic gates based on Boolean algebra principles. There are two primary types of digital comparators on the market:

1. **Identity Comparator:** An identity comparator is a digital comparator with only one output terminal for when $A = B$, either $A = B = 1$ (HIGH) or $A = B = 0$ (LOW)

2. **Magnitude Comparator:** In general a magnitude digital comparator is a combinational circuit which is used to compare two binary numbers in order to find out whether one binary number is equal, less than or greater than the other binary number.

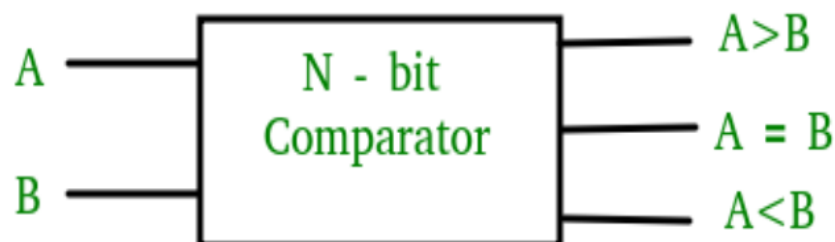


Figure 8.1: Block diagram of N bit magnitude digital comparator.

(L)

In an N bit magnitude digital comparator will have inputs such as A and B and outcome of the comparator is specified by three binary variables that indicate whether $A > B$, $A = B$ or $A < B$.

1-Bit Magnitude Comparator –

A comparator used to compare two bits is called a single bit comparator or 1-Bit Magnitude Comparator. It consists of two inputs each for two single bit numbers and three outputs to generate less than, equal to and greater than between two binary numbers.

The truth table for a 1-bit comparator is given below:

A	B	$A < B$	$A = B$	$A > B$
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Table 8.2: Truth table for a 1-bit comparator.

From the above truth table logical expressions for each output can be expressed as follows:

Boolean Expression:

$$A > B = \bar{A}B$$

$$A < B = A\bar{B}$$

$$A = B = A\bar{B} + \bar{A}B$$

For $A = B$ we will use X-NOR gate.

By using these Boolean expressions, we can implement a logic circuit for this comparator as given below:

(L)

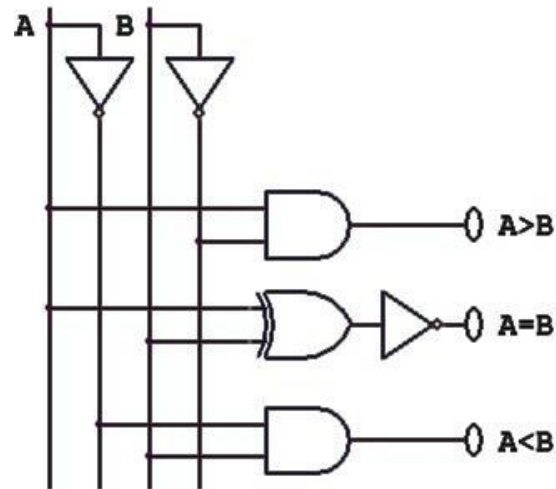


Figure 8.3: Logic implementation of 1-Bit Magnitude Comparator.

2-Bit Magnitude Comparator –

A comparator used to compare two binary numbers each of two bits is called a 2-bit magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to and greater than between two binary numbers.

(L)

INPUT				OUTPUT		
A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Figure 8.4:The truth table for a 2-bit comparator.

For finding out the Boolean expression for the above mentioned truth table. We will from K-map for each output as given below:

(L)

		A>B			
		B1B0 00	01	11	10
A1A0	00	0	0	0	0
	01	1	0	0	0
	11	1	1	0	1
	10	1	1	0	0

Figure 8.5: K-map for A>B expression.

		A=B			
		B1B0 00	01	11	10
A1A0	00	1	0	0	0
	01	0	1	0	0
	11	0	0	1	0
	10	0	0	0	1

Figure 8.6: K-map for A=B expression.

(L)

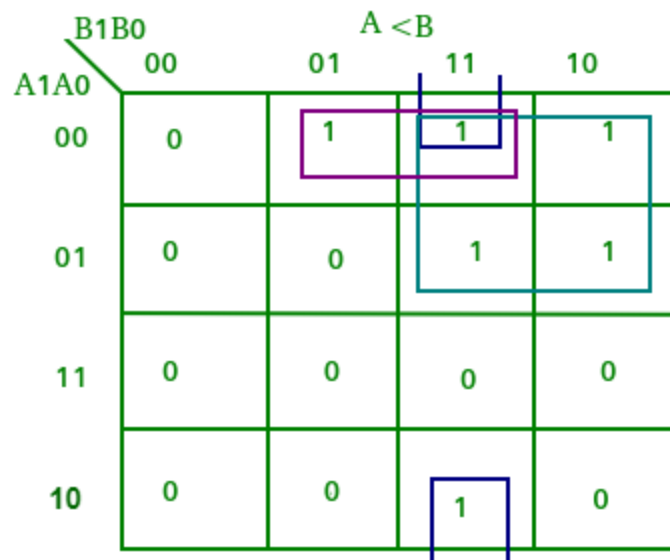


Figure 8.7: K-map for $A < B$ expression.

From the above K-maps logical expressions for each output can be expressed as follows:

$A > B$

$$: A1B1' + A0B1'B0' + A1A0B0'$$

$A = B$

$$: A1'A0'B1'B0' + A1'A0'B1'B0 + A1A0B1B0 + A1A0'B1B0'$$

$$: A1'B1'(A0'B0' + A0B0) + A1B1(A0B0 + A0'B0')$$

$$: (A0B0 + A0'B0')(A1'B1' + A1B1)$$

$$: (A0 \text{ Ex-Nor } B0) (A1 \text{ Ex-Nor } B1)$$

$A < B$

$$: A1'B1 + A0'B1B0 + A1'A0'B0$$

By using these Boolean expressions, we can implement a logic circuit for this comparator as given below:

(L)

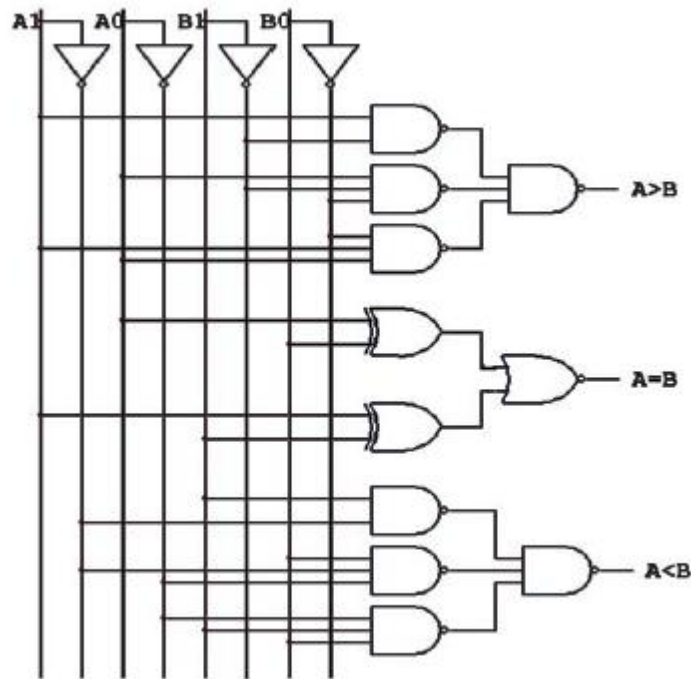


Figure 8.7: logic circuit for logic circuit for two bit magnitude comparator.

Applications of Comparators –

There are a number of applications of magnitude comparators some of them are mentioned below:

1. Magnitude comparators are used in central processing units (CPUs) and microcontrollers (MCUs).
2. Comparators are also used in biometric applications.
3. These are used in password verification.
4. These are used in control applications in which the binary numbers representing physical variables such as temperature, position, etc. are compared with a reference value.
5. Comparators are also used as process controllers and for Servo motor control.

(L)

Pin Diagram For IC 7485

Detail pin diagram for IC 7485 is shown in the below figure. In this IC, Pin number 16 is Vcc, Pin 8 is ground, Pin 5, 6, 7 are outputs and Pin 9, 10, 11, 12, 13, 14, 15 are inputs.

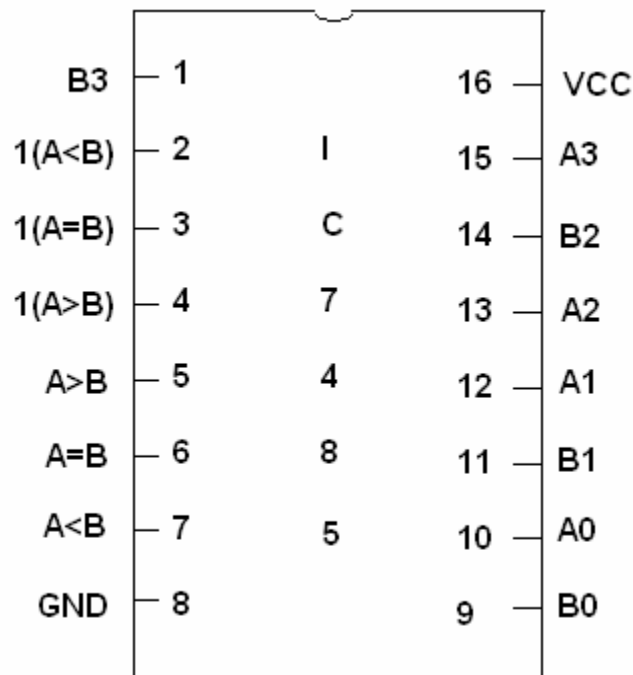


Figure 8.8:Pin Diagram for IC 7485.

8.5 PROCEDURE

- (i) Verify the gates
- (ii) Connections are given as per circuit diagram.
- (iii) Logical inputs are given as per circuit diagram.
- (iv) Observe the output and verify the truth table.

(L)

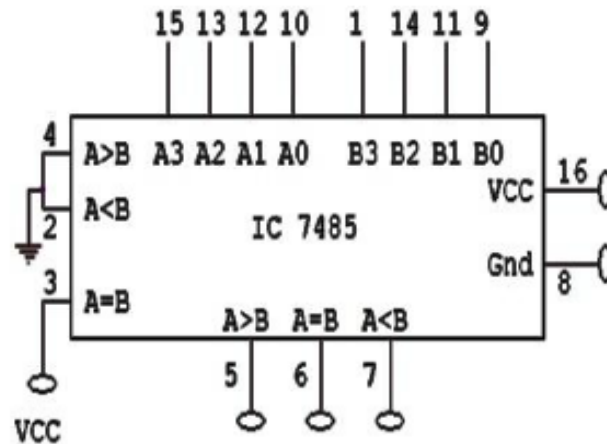


Figure 8.8: Logic Diagram of Magnitude Comparator

1- Bit Magnitude Comparator

Step-1) Switch ON the power supply button to supply 5V to the circuit.

Step-2) Press Switch 1 for input A and Switch 2 for input B.

The switch in ON state and the switch in OFF state

Step-3) i)When the input A is greater than the input B,LED 5lits up.

ii)When the input A is lesser than the input B,LED 7 lits up.

iii)When the input A is equal to the input B,LED 6 lits up.

2- Bit Magnitude Comparator

Step-1) Switch ON the power supply button to supply 5V to the circuit.

Step-2) Press Switch 1 for input A1,Switch 2 for input A0,Switch 3 for input B1and Switch 4 for input B0.

The switch in ON state and the switch in OFF state

Step-3) i)When the input A1A0 is greater than the input B1B0,LED 5lits up.

(L)

ii)When the input A1A0 is lesser than the input B1B0,LED 7lights up.

iii)When the input A1A0 is equal to the input B1B0,LED 6lights up.

8.6 RESULTS

The Truth Table and output is verified.

8.7 PRECAUTION AND SOURCE OF ERROR

- IC should be checked before stating the experiment.
- All connection should be tight.
- Connect the ground first then connect the Vcc.
- Main voltage should be kept switched off, while making connections.
- Digital kit should be handled with utmost care.
- Circuit should be off before change the connections.
- We should switch off the power supply after completing experiment.
- We should not touch the naked wire.

8.8 GLOSSARY

Input	An input is data that a computer receives.
Output	An output is data that a computer sends.
Digital	Electronic technology that uses discrete values, generally zero and one, to generate, store and process data.
Comparator	An electronic circuit for comparing two electrical signals.
Boolean algebra	It is the branch of algebra in which the values of the variables are the truth values true and false, usually denoted 1 and 0, respectively.
Bit	The smallest increment of data on a computer
Binary	The digits 0 and 1 - to store data
IC	An assembly of electronic components, fabricated as a single unit, in which miniaturized active devices

(L)

8.9 VIVA-VOCE QUESTIONS AND ANSWERS

1. What is a comparator?

Answer: A digital magnitude comparator is a combinational circuit that compares two digital or binary values to see if one is equal to, less than, or greater than the other.

2. What are the applications of comparator?

Answer: The digital comparators are employed in a variety of applications where data comparison is required for a variety of tasks, and they have a number of advantages.

- Examine a handful of the applications for comparators that are used for authorisation (such as password management) and biometric applications.
- These are used in servo motor controls as well as process controllers.
- The pressure is compared to those of reference values for data comparison of variables such as temperature.
- Computer decoding circuitry is addressed using this term.

3. How many inputs are required for a digital comparator?

Answer: A comparator takes two numbers as input in binary form and results whether one input is greater, lesser or equal to the other input. Thus there are two inputs required for a digital comparator.

4. Which logic gate is known as basic comparator?

Answer: XNOR gate is known as basic comparator.

5. How many types of digital comparators are?

Answer: There are mainly two types of Digital Comparator. These are Identity comparator and Magnitude comparator.

(L)

8.10 REFERENCES

1. William Gothmann H, Digital Electronics : An Introduction To Theory And Practice , Prentice Hall, 2nd ed. 1982
2. M. Morris Mano, Michael D Ciletti, "Digital Design", Pearson, 4th ed. 2008
3. Thomas L. Floyd, R. P. Jain, "Digital Fundamentals", Pearson, 11th ed. 2017
4. S Salivahanan, S Arivazhagan, "Digital Circuits and Design", Vikas Publishing House Pvt Ltd., 3rd ed. 2009
5. Ronald J. Tocci, Neal S. Widmer, Gregory L. Moss, "Digital Systems", Pearson, 10th ed. 2009
6. Anil K. Maini, "Digital Electronics: Principles, Devices and Applications", Wiley-Blackwell, 2007
7. 1 Bit comparator: <https://www.youtube.com/watch?v=UO-K0Jx2Hs0>
8. Magnitude Comparator: <https://www.geeksforgeeks.org/magnitude-comparator/>
9. Digital Comparator and Magnitude Comparator: <https://www.electronicshub.org/digital-comparator-and-magnitude-comparator/>